SD8709

2 Diff Channels ADC SOC with RTC and 24*4 LCD

Features

- High precision ADC, ENOB=18.8bits@8sps, 2 differential or 4 single-ended inputs
- Low noise, high input impedance preamplifier with selectable gain: 1, 12.5, 50, 100, or 200
- 8 bits RISC ultra-low power MCU. The MCU current consumption is 300uA typically at 3V and 2MHz operating clock rate. Standby current is 1.5uA at 32kHz clock, and less than 1uA at sleep
- 16K Bytes OTP, 512 Bytes SRAM
- Low OTP programming voltage, can replace external EEPROM
- Multiple clock sources, flexible clock selection, external oscillator malfunction detection
- ADC output rate: 8SPS–2kSPS
- 24SEG X 4COM LCD drive, ultra-low power consumption and high driving capability, programmable boost module to maintain luminance at low supply voltage
- Built-in temperature sensor, supports single point calibration
- 1.2V low temperature drift voltage reference output
- Selectable voltage source for external transducer excitation: 2.4V/2.6V/2.9V/3.3V
- Flexible battery voltage detection range 2.0V~ 3.3V
- External or internal voltage reference for ADC, multiple internal voltage references
- RTC module provides second output
- Abundant peripheral resources: UART, I^2C, SPI, PWM/PDM, PFD, TIMER, CAPTURE
- Low voltage detection and power on reset circuit
- Operating voltage range: 2.4V~ 3.6V
- Operating temperature range: -40 ˚C~85 ˚C

Description

The SD8709 is a CMOS SOC with built-in 24 bit ADC and abundant peripheral resources: RTC, selectable voltage sources, flexible PGIA, voltage step-up module, UART, I^2C, SPI, TIMER, PWM/PDM, PFD, CAPTURE, and LCD driver.

The OTP can be programmed in situ and the 2.4V~3.6V programming voltage is generated internally. The OTP can be used in place of external EEPROM.

The IC was designed with ultra-low power technology. Typical total operating current is only 1mA (IAD=0) or 1.5mA (IAD=1).

Three working modes are provided so users can select the optimum choice between speed and power. They are normal mode, standby mode, and sleep mode.

Applications

Infrared temperature measurement, instrument and meter, weak transducer signal processing applications

Ordering Information

QFN48 package

Pin Diagram and Descriptions

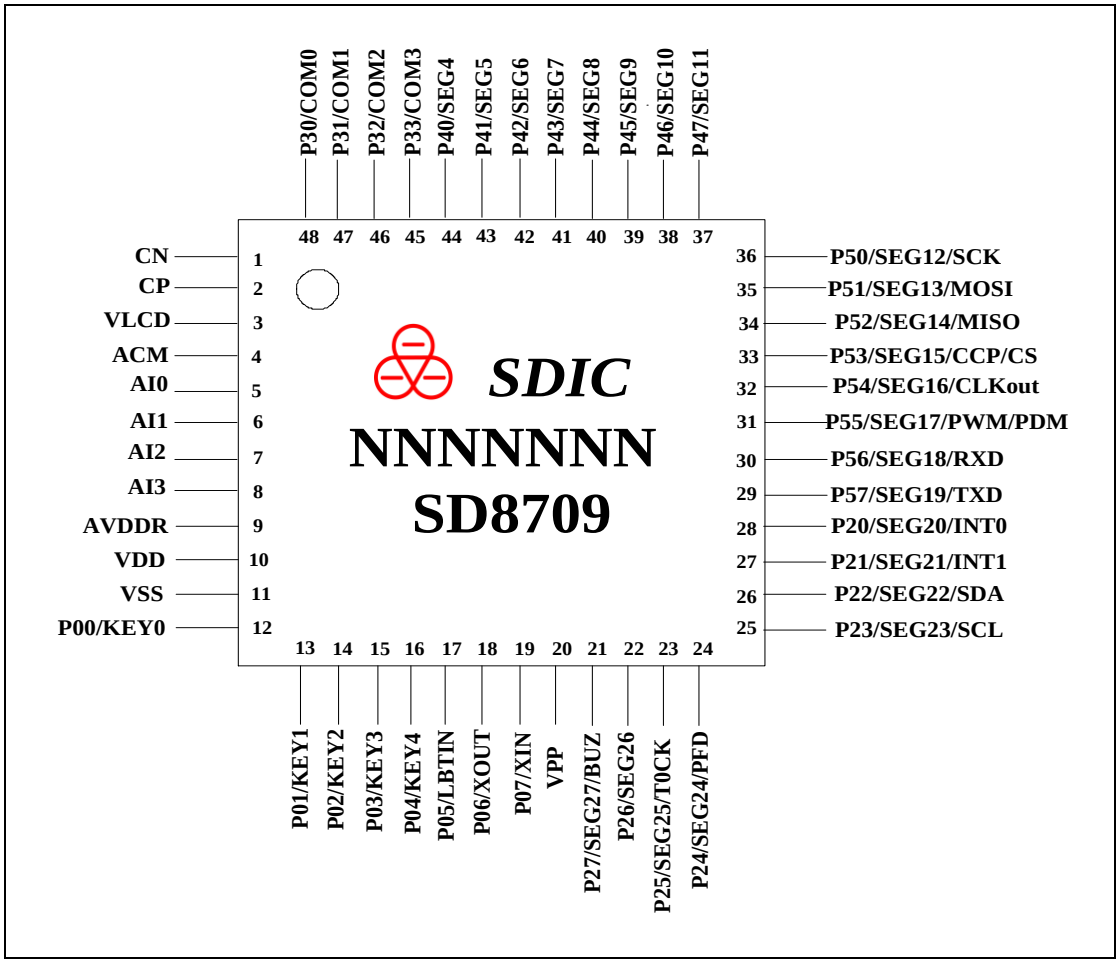


Figure 1. Pad diagram

Table 1. Pad Descriptions

Pad No.	Pin Name	Attribute	Description
1-2	CN, CP	Analog	External capacitor connection pins for the voltage booster circuit. Capacitor not needed if high frequency RC clock is used for the booster
3	VLCD	Analog	LCD driver power supply, internally connect to VDD or booster output through register setting, connect 1uF filter capacitor to VDD
4	ACM	Analog	1.2V reference output, floating when ACM is shutdown, connect 0.1uF cap to VSS
5-8	AI0 -- AI3	Analog input	Analog signal inputs, each port has an independent register controlled pull-down resistor (default OFF), should set to ON for unused port; AI0-1, AI2-3 can be used as 2 differential or 4 single-ended inputs
9	AVDDR	Analog	Internal LDO output for IC's analog module, can provide excitation to external transducer, connect 0.1uF to 10uF filter capacitor to VSS
10	VDD	Power	Power supply voltage, connect 0.1uF capacitor to VSS
11	VSS	Ground	Power ground

12-16	P00/KEY0 -- P04/KEY4	I/O	Digital port P00-04 or external key inputs KEY0-4
17	P05/LBTIN	Analog , I/O	Digital port P05 or low battery detect LBTIN input
18-19	P06/XOUT -- P07/XIN	Analog , I/O	Digital ports P06-07, or 32.768kHz or 1MHz-4MHz crystal oscillator pins XIN can be used as external clock input
20	VPP	I	OTP high voltage programming pin, connect 1uF capacitor to VSS
21	P27/SEG27/ BUZ	I/O	Digital port P27, LCD segment SEG27, or buzzer BUZ output
22	P26/SEG26	I/O	Digital port P26 or LCD segment SEG26
23	P25/SEG25/ T0CK	I/O	Digital port P25, LCD segment SEG25, or TIMER0 external clock T0CK input
24	P24/SEG24/ PFD	I/O	Digital port P24, LCD segment SEG24, or Programmable frequency divider PFD
25	P23/SEG23/SCL	I/O	Digital port P23, LCD segment SEG23, or I^2C clock line
26	P22/SEG22/SDA	I/O	Digital port P22, LCD segment SEG22, or I^2C data line
27	P21/SEG21/INT1	I/O	Digital port P21, LCD segment SEG21, or external interrupt INT1
28	P20/SEG20/INT0	I/O	Digital port P20, LCD segment SEG20, or external interrupt INT0
29-30	P57/SEG19/TXD-- P56/SEG18/RXD	I/O	Digital port P57-56, LCD segment SEG19-18, or UART data transmit TXD and data receive RXD
31	P55/SEG17/ PWM/PDM	I/O	Digital port P55, LCD segment SEG17, or PWM/PDM output
32	P54/SEG16/CLKout	I/O	Digital port P54, LCD segment SEG16, or CLKout output
33	P53/SEG15/CCP/CS	I/O	Digital port P53, LCD segment SEG15, compare/capture output CCP, or SPI's CS port
34	P52/SEG14/MISO	I/O	Digital port P52, LCD segment SEG14, or SPI's MISO port
35	P51/SEG13/MOSI	I/O	Digital port P52, LCD segment SEG13, or SPI's MOSI port
36	P50/SEG12/SCK	I/O	Digital port P50, LCD segment SEG12, or SPI's SCK port
37-44	P47/SEG11-- P40/SEG4	I/O	Digital port P47-40 or LCD segment SEG11-4
45-48	P33/COM3-- P30/COM0	I/O	Digital port P33-30 or LCD COM3-0 During serial programming, COM3-0 serve as Data Output, 2MHz clock Input, Data Input, and Data Clock

Remark:

1. All I/O ports Pnn have internal pull-up option (default OFF) and input hysteresis at 0.3VDD/0.7VDD.

Functional Block

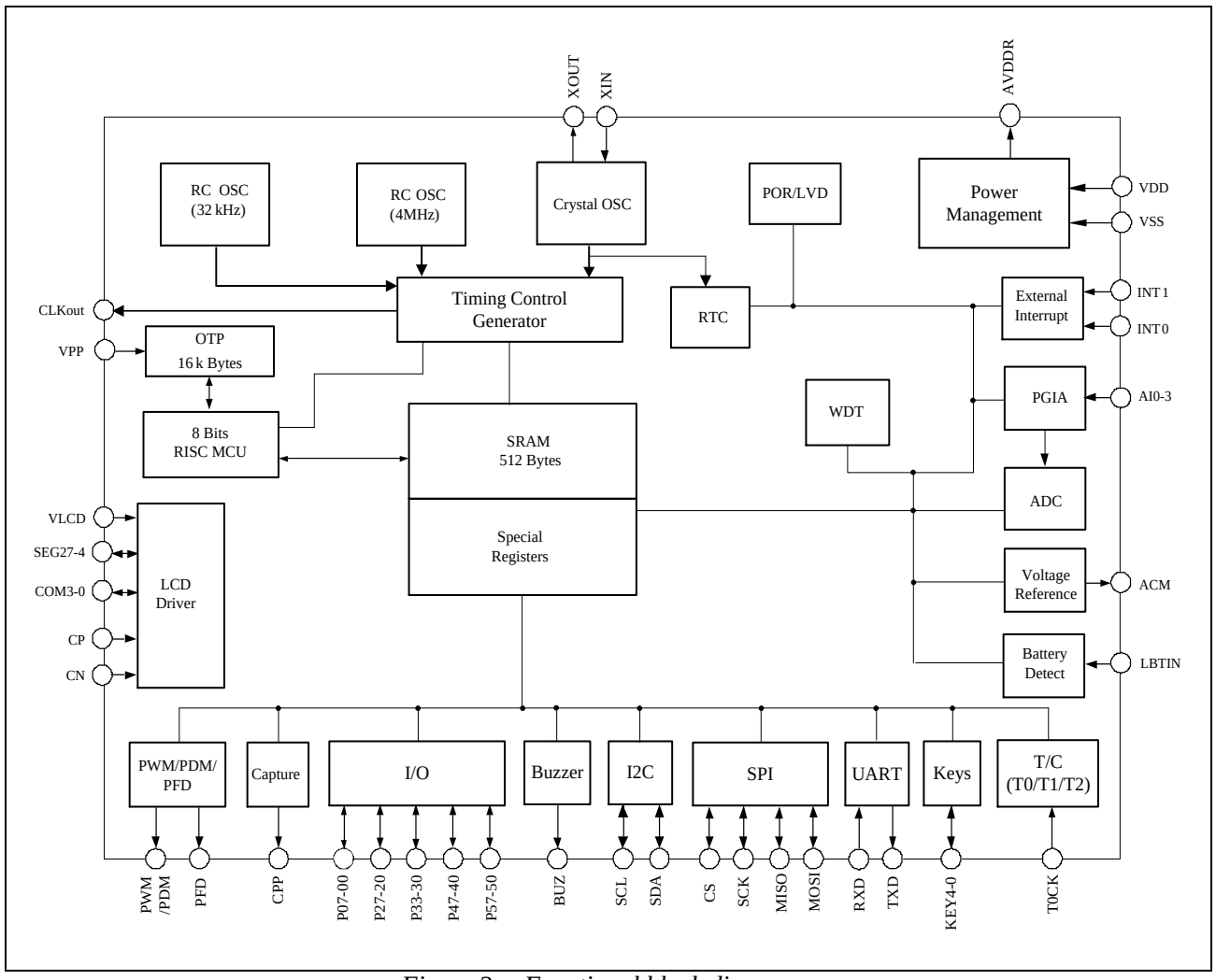


Figure 2. Functional block diagram

Typical Applications

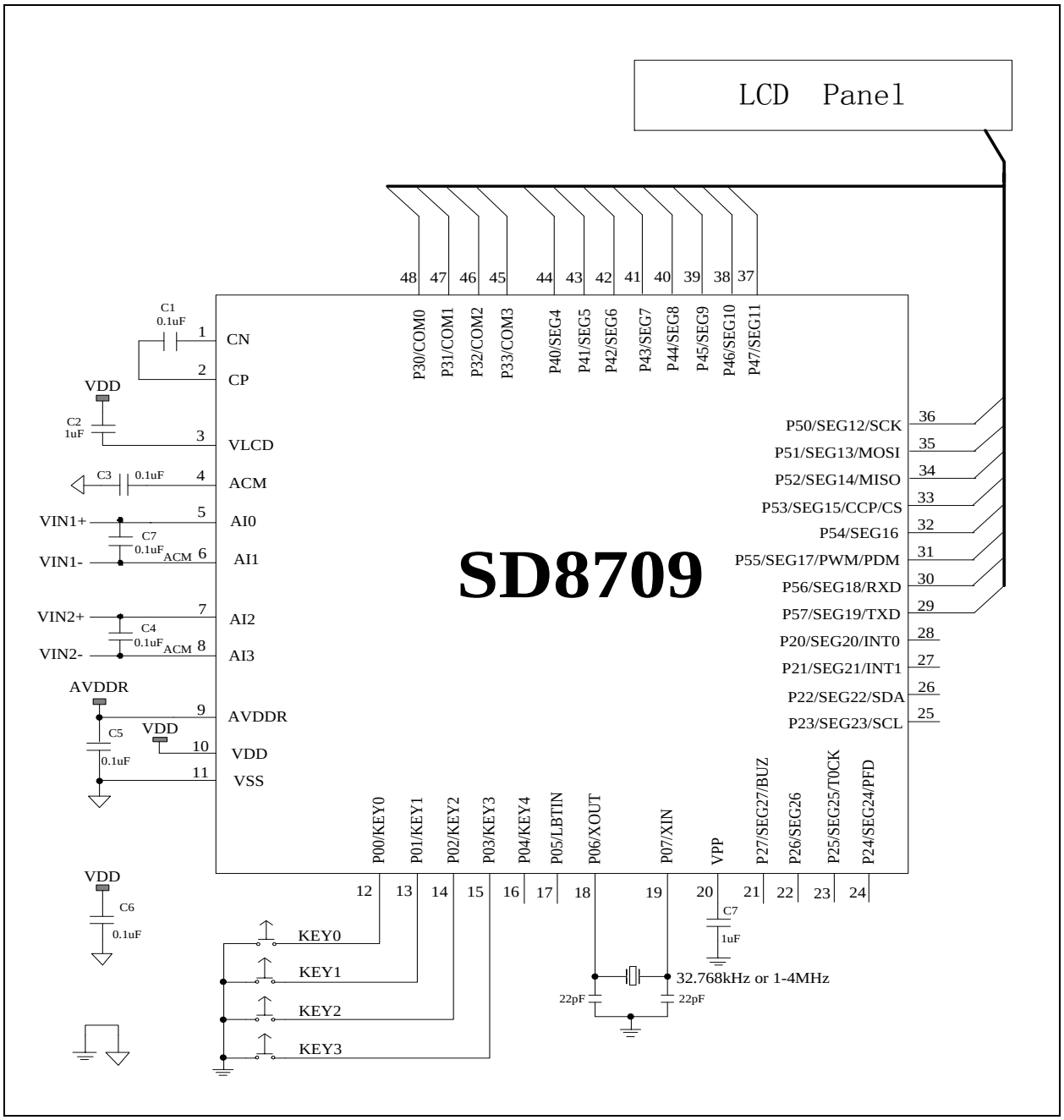


Figure 3. Weak transducer signal measurement typical application diagram

ADC Characteristics

Table 2. ENOB and voltage noise Vn_{rms} (AVDDR=2.4V, VREF=0.6V, SINC3, Buffer on, IAD=1)

ADC sampling rate = 128kHz										
OSR			128	256	512	1024	2048	4096	8192	16384
Gain	200	**ENOB**	14.7	15.2	15.7	16.1	16.6	17.1	17.5	18.0
		Vn_{rms}(nV)	227	162	116	83	59	42	32	22
	100	**ENOB**	15.4	16.0	16.5	17.0	17.4	17.9	18.4	18.8
		Vn_{rms}(nV)	269	190	133	94	68	49	35	27
	1	**ENOB**	16.3	16.9	17.4	17.9	18.3	18.6	19.2	19.5
		Vn_{rms}(nV)	15027	9924	7079	5078	3640	3235	2067	1656

ADC sampling rate = 512kHz										
OSR			128	256	512	1024	2048	4096	8192	16384
Gain	200	**ENOB**	--	14.2	14.7	15.2	15.7	16.2	16.6	17.1
		Vn_{rms}(nV)	--	319	224	160	113	80	59	44
	100	**ENOB**	--	15.0	15.5	16.0	16.5	17.0	17.4	17.8
		Vn_{rms}(nV)	--	364	256	183	128	94	70	55
	1	**ENOB**	--	16.0	16.5	16.9	17.4	17.8	18.1	18.3
		Vn_{rms}(nV)	--	18317	12953	9614	6953	5303	4347	3860

Remark:

The above data are averages based on multiple ICs' measured results. Each IC contributes 1024 data points.

ENOB = $\log_2(\frac{FRS}{Vrms})$, FRS is the Full Scale Voltage Range (2 * Vref / Gain), Vrms is the rms Noise.

Electrical Specifications

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
T_A	Operating temperature	-40	+85	℃
T_S	Storage temperature	-55	+150	℃
V_{DD}	Supply voltage	-0.2	+4.0	V
Vpp	Programming voltage	-0.2	+7.5	V
V_{IN}, V_{OUT}	Digital input/output voltage	-0.2	V_{DD}+0.3	V
T_L	Reflow temperature profile	Per IPC/JEDECJ-STD-020C		℃

Remarks:

1. CMOS device can easily be damaged by electrostatics. It must be stored in conductive foam, and careful not to exceed the operating voltage range.
2. Turn off power before insert or remove the device.

Table 4. Electrical Specifications（VDD=3V, T_A=25℃）

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Remarks
VDD	Supply voltage	2.4	3.0	3.6	V	Analog modules operating voltage
		2.0	3.0	3.6	V	Digital modules and MCU operating voltage
FOSC	Operating frequency	16k	2M	4M	Hz	FOSC must be 2MHz when read/write tables in OTP
IHRC	Internal high frequency RC oscillator	--	4	--	MHz	Frequency after calibration
ILRC	Internal low frequency RC oscillator	28	--	36	kHz	Frequency after calibration
HXT	External high frequency crystal oscillator	1	--	4	MHz	
LXT	External low frequency crystal oscillator	16	32.786	--	kHz	
IDD1	Operating current 1	--	1.5	--	mA	Internal RC oscillator freq halved for MCU Analog modules active, IAD=1
IDD2	Operating current 2	--	1	--	mA	Internal RC oscillator freq halved for MCU Analog modules active, IAD=0
IDD3	Operating current 3	--	1.5	--	uA	32kHz internal RC oscillator for MCU MCU at standby mode Analog modules inactive
IDD4	Operating current 4	--	1	--	uA	MCU at sleep mode Analog modules inactive
Fsam	ADC sampling rate	--	128	512	kHz	
OSR	Over sampling rate	128	--	65536		
NFbit	Noise free bits[1]	--	16	--	bits	Gain=200, input FSR=±4mV
NMbit	No missing code	--	--	24	bits	
INL	INL	--	0.002	--	%FSR	
VINdif	PGIA differential input range	-Vref	--	Vref	mV	1X gain
		-Vref/12.5	--	Vref/12.5		12.5X gain
		-Vref/50	--	Vref/50		50X gain
		-Vref/100	--	Vref/100		100 X gain

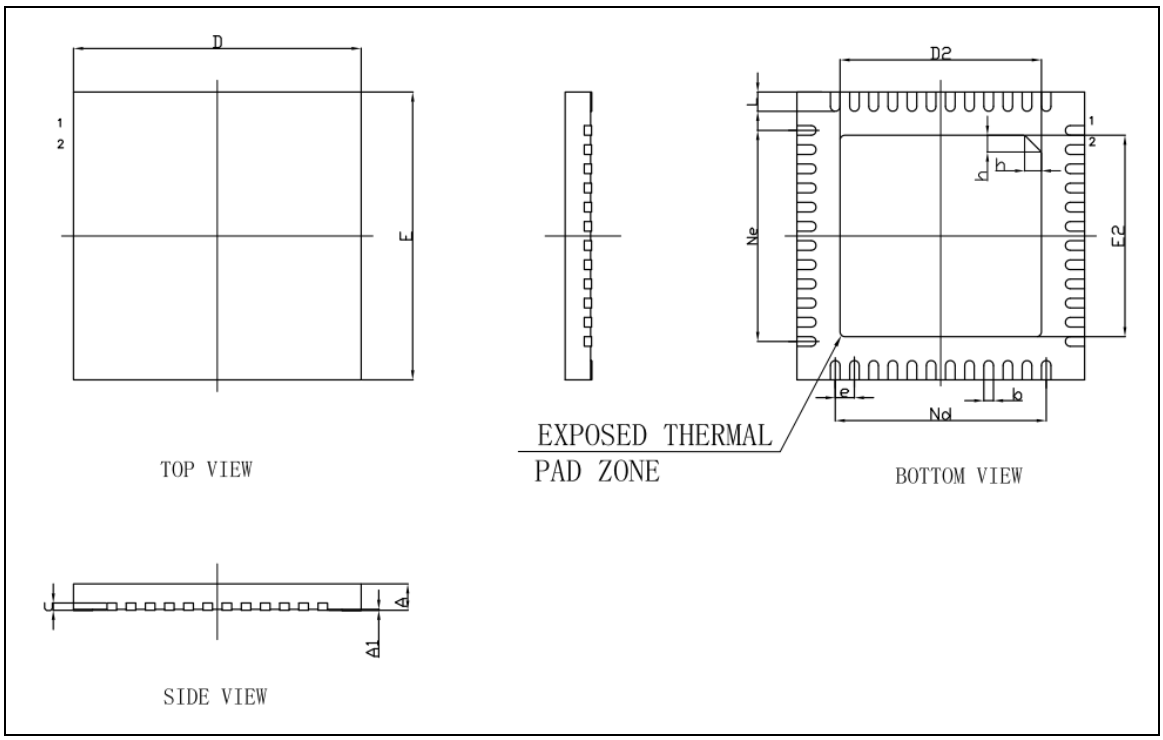
		-Vref/200	--	Vref/200		200 X gain
VIN	PGIA input voltage range[2]	-0.3	--	AVDDR		1X gain and buffer is off
		0.3	--	AVDDR-0.7		1X gain and buffer is on, or gain≠1
Vnrms	RMS noise	--	22	--	nVrms	200X gain
Vacm	ACM voltage output	--	1.2	--	V	
IacmSour	ACM current source	--	1	--	mA	
IacmSink	ACM current sink	--	1	--	mA	
PSRacm	ACM PSR	--	100	--	uV/V	
Tgain	Gain tempco	--	±4	--	ppm/℃	-10℃ to +40℃
Vavddr	AVDDR voltage output	--	2.4	--	V	AVDDRX [1:0]=00
		--	2.6	--		AVDDRX [1:0]=01
		--	2.9	--		AVDDRX [1:0]=10
		--	3.3	--		AVDDRX [1:0]=11
Iavddr	AVDDR current	--	10	--	mA	
POR	POR voltage	--	2.0	--	V	
LVD	LVD voltage	--	1.9	--	V	
THlbt	LVD hysteresis	--	200	--	mV	
Vlbt	Low VDD alarm threshold	--	3.3	--	V	LBTX[3:0]=0010
		--	3.2	--		LBTX[3:0]=0011
		--	3.1	--		LBTX[3:0]=0100
		--	3.0	--		LBTX[3:0]=0101
		--	2.9	--		LBTX[3:0]=0110
		--	2.8	--		LBTX[3:0]=0111
		--	2.7	--		LBTX[3:0]=1000
		--	2.6	--		LBTX[3:0]=1001
		--	2.5	--		LBTX[3:0]=1010
		--	2.4	--		LBTX[3:0]=1011
		--	2.3	--		LBTX[3:0]=1100
		--	2.2	--		LBTX[3:0]=1101
		--	2.1	--		LBTX[3:0]=1110
		--	2.0	--		LBTX[3:0]=1111
Vlcd	LCD charge pump output voltage	--	2.1	--	V	VLCDX[2:0]=000
		--	2.3	--		VLCDX[2:0]=001
		--	2.5	--		VLCDX[2:0]=010
		--	2.7	--		VLCDX[2:0]=011
		--	2.9	--		VLCDX[2:0]=100
		--	3.1	--		VLCDX[2:0]=101
		--	3.3	--		VLCDX[2:0]=110
		--	3.5	--		VLCDX[2:0]=111
Ilcd	LCD charge pump current[3]	--	--	500	uA	

Digital I/O parameter						
IOH	High output current source	--	3	--	mA	VOH=VDD-0.3V, PTxSR=0
		--	12	--		VOH=VDD-0.3V, PTxSR=1
IOL	Output low current sink	--	3	--	mA	VOL=0.3V, PTxSR=0
		--	12	--		VOL=0.3V, PTxSR=1
VIH	Input high voltage	0.7VDD	--	--	V	
VIL	Input low voltage	--	--	0.3VDD	V	
VOH	Output high voltage	VDD-0.3	--	--	V	
VOL	Output low voltage	--	--	VSS+0.3	V	
Rpu	Pin pull up resistance	--	50	--	kΩ	VDD = 3.0

Note:

1. Noise free bits and effective resolution are both related to the signal's full scale range. Its peak to peak or rms noise plays the decisive role.
2. The signal input range is limited by the differential signal input range and the absolute voltage at the input terminals. The first one is the real signal input range. It is affected by the PGIA gain and the ADC voltage reference choice. The second one includes both differential and common mode components and is mainly limited by the circuit.
3. The charge pump driving capability is related to the choice of capacitor and the operating frequency.

Packaging Information



Dimensions: mm

Symbol	Min.	Nom.	Max.
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.10	0.15	0.20
D	5.90	6.00	6.10
D2	4.10	4.20	4.30
e	0.40BSC		
Ne	4.40BSC		
Nd	4.40BSC		
E	5.90	6.00	6.10
E2	4.10	4.20	4.30
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Figure 4. QFN48 mechanical specification