SD8304

20 bits ADC SOC with RTC, UART, and LCD Drivers

Features

- High precision ADC, ENOB=17.3bits@8sps, 1 differential or 3 single-ended inputs
- Low noise, high input impedance preamplifier with selectable gain: 1, 12.5, 50, 100, or 200
- 8 bits RISC ultra-low power MCU, 49 instructions and 6 stack levels. The MCU current consumption is 400uA typically at 3V and 2MHz operating clock rate, 1uA at standby and 32kHz clock, and less than 1uA at sleep
- 16k Bytes OTP, 256 Bytes SRAM
- Low OTP programming voltage at 2.4~3.6V, can replace external EEPROM
- Built-in oscillator. Provides second, minute, hour data when 32.768kHz crystal is connected
- 8 bits TIMER for timing interrupts, support PFD output
- Built-in temperature sensor, supports single point calibration
- 20SEG X 4COM LCD drive, programmable boost module to maintain luminance at low supply voltage
- LCD driver supports 1/2BIAS and 1/3BIAS modes
- Selectable voltage source for external transducer excitation: 2.4V/2.6V/2.9V/3.3V
- Flexible battery voltage detection: 2.4V~3.0V
- Schmitt trigger input, pull up resistor selectable
- Watch Dog Timer
- Low voltage detection and power on reset circuit
- Operating voltage range: 2.4V~3.6V
- Operating temperature range: -40˚C~85 ˚C

Description

The SD8304 is a CMOS SOC with built-in 20 bits ADC and 16k Bytes OTP memory. The built-in OTP has low programming voltage at 2.4V~3.6V. It can be used in place of external EEPROM. The IC is specially designed for domestic use body weight scale or health scale. Only five external capacitors are needed when using this IC.

The IC was designed with ultra-low power technology. Operates at 3V supply and halved internal RC oscillator frequency, the total typical operating current is 800uA (external transducer driving current not included). Such low current consumption is very suitable for battery powered applications.

Three working modes are provided so users can select the optimum choice between speed and power. They are normal mode, standby mode, and sleep mode.

Applications

Health scale, body weight scale, kitchen scale, palm scale, portable scale

Ordering Information

QFN40 package

Pin Diagram and Descriptions

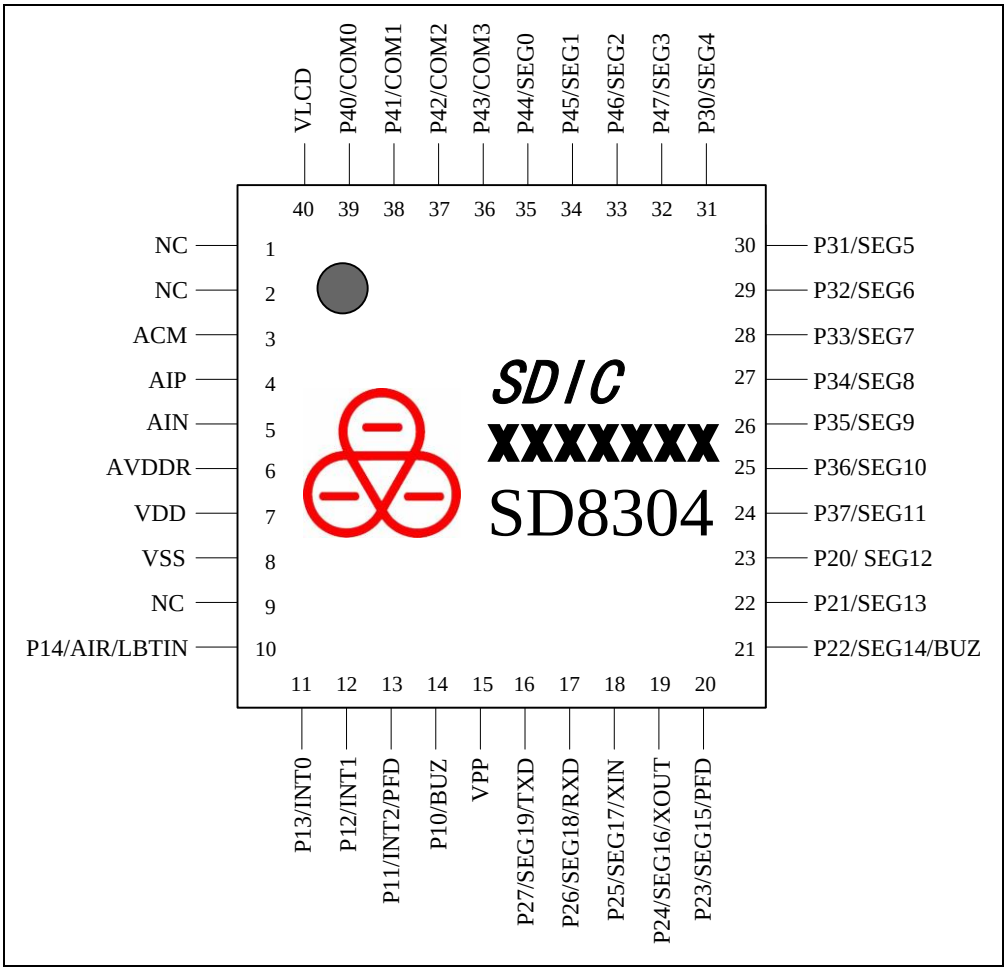


Figure 1. Pad diagram

Table 1. Pad Descriptions

Pad No.	Pin Name	Attribute	Description
1	NC	--	--
2	NC	--	--
3	ACM	Analog	1.2V reference output, floating when ACM is shutdown, connect 0.1uF cap to VSS
4	AIP	Analog	Analog signal differential inputs Should enable the internal pull-down resistor for unused input
5	AIN	Analog	
6	AVDDR	Analog	Internal LDO output for IC's analog module, can provide excitation to external transducer, connect 0.1uF filter capacitor to VSS
7	VDD	Power	Power supply voltage, connect 0.1uF capacitor to VSS
8	VSS	Ground	Power ground
9	NC	--	--
10	P14/AIR/LBTIN	I/O/ Analog	Digital port P14, analog signal or reference voltage input with respect to VSS, or low battery detect LBTIN input
11	P13/INT0	I/O	Digital port P13 or external interrupt INT0
12	P12/INT1	I/O	Digital port P12 or external interrupt INT1
13	P11/INT2/PFD	I/O	Digital port P11, external interrupt INT2, or PFD output
14	P10/BUZ	I/O	Digital port P10 or buzzer BUZ output
15	VPP	I	OTP high voltage programming pin, connect 1uF capacitor to VDD or VSS
16	P27/SEG19/TXD	I/O	Digital port P27, LCD segment SEG19, or UART data transmit TXD
17	P26/SEG18/RXD	I/O	Digital port P26, LCD segment SEG18, or UART data receive RXD
18	P25/ SEG17/XIN	I/O	Digital port P25, LCD segment SEG17, or crystal oscillator input XIN
19	P24/SEG16/XOUT	I/O	Digital port P24, LCD segment SEG16, or crystal oscillator output XOUT
20	P23/SEG15/PFD	I/O	Digital port P23, LCD segment SEG15, or PFD output
21	P22/SEG14/BUZ	I/O	Digital port P22, LCD segment SEG14, or buzzer BUZ output
22-23	P21/SEG13-- P20/ SEG12	I/O	Digital port P21-20 or LCD segment SEG13-12
24-31	P37/SEG11-- P30/ SEG4	I/O	Digital port P37-30 or LCD segment SEG11-4
32-35	P47/SEG3-- P44/ SEG0	I/O	Digital port P47-44 or LCD segment SEG3-0
36-39	P43/COM3-- P40/ COM0	I/O	Digital port P43-40 or LCD COM3-0
40	VLCD	Analog	LCD driver power supply, internally connect to VDD or booster output through register setting, connect 1uF filter capacitor to VDD

Remark: All I/O ports Pnn have internal pull-up option (default OFF) and input hysteresis at 0.3VDD/0.7VDD.

Functional Block

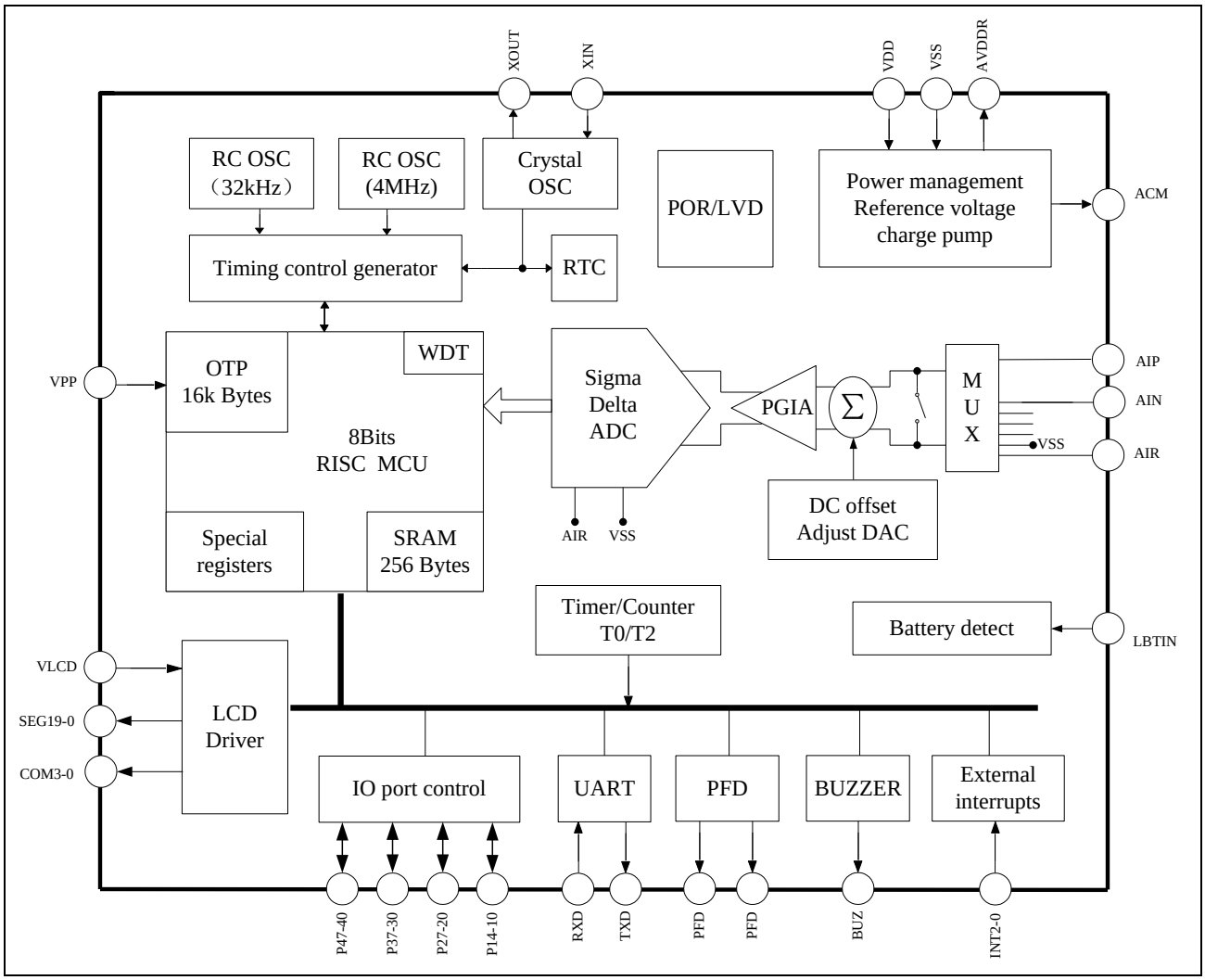


Figure 2. Functional block diagram

Typical Application

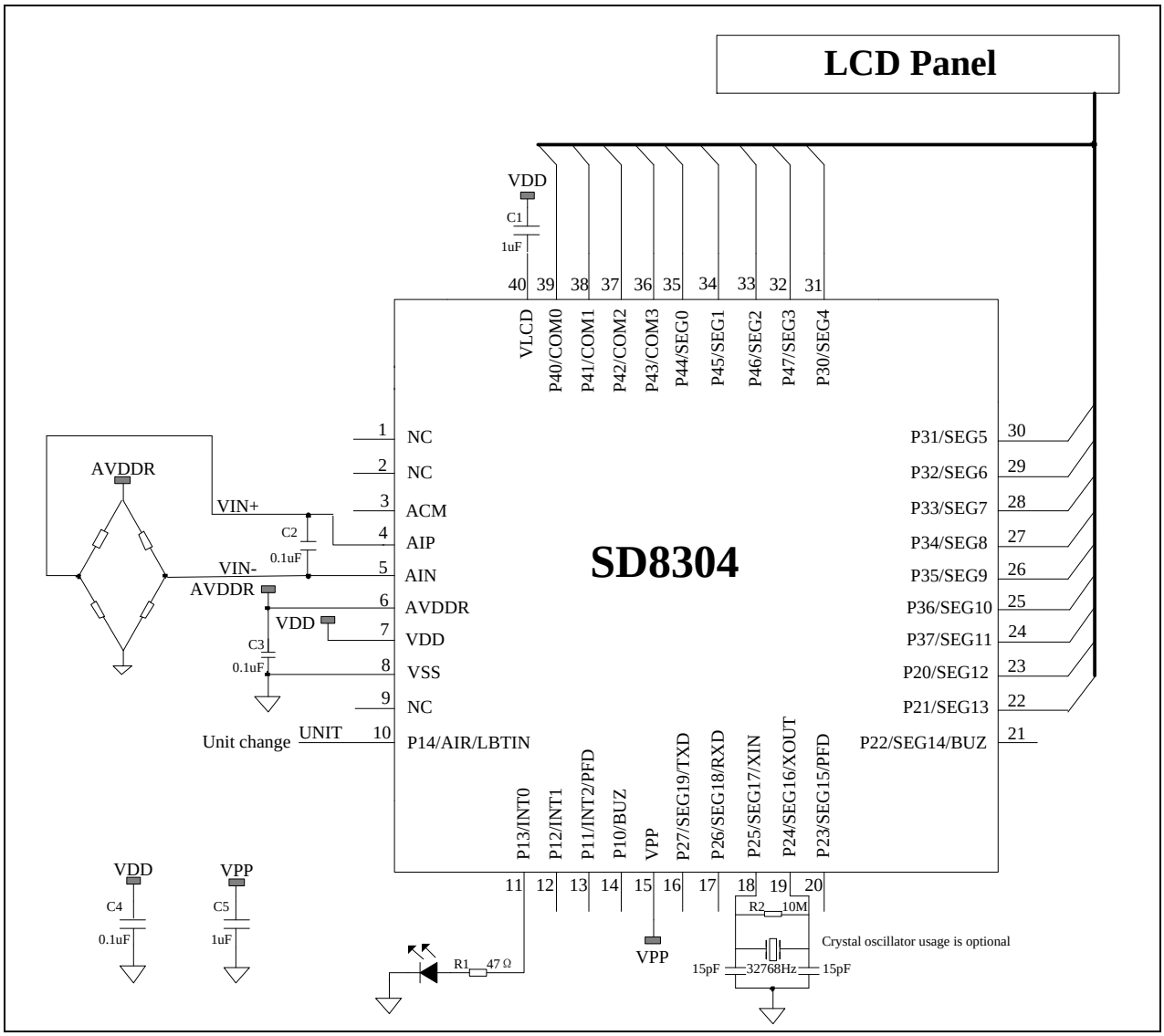


Figure 3. LCD Body scale with time display typical application diagram

ADC Characteristics

Table 2. ENOB and voltage noise Vn_{rms} (AVDDR=2.4V, VREF=0.6V, SINC3, Buffer on)

ADC sampling rate = 128kHz										
OSR			128	256	512	1024	2048	4096	8192	16384
Gain	200	**ENOB**	13.7	14.3	14.9	15.4	15.9	16.4	16.8	17.3
		Vn_{rms}(nV)	526.5	305.2	198.8	143.1	102.5	72.1	51.6	38.8
	100	**ENOB**	14.9	15.4	15.9	16.3	16.8	17.3	17.8	18.3
		Vn_{rms}(nV)	402.3	283.3	204.1	146.6	104.4	75	53.9	38.5
	1	**ENOB**	16.3	17	17.4	17.7	18.1	18.8	19.5	20.3
		Vn_{rms}(nV)	14677.9	9520.5	7147.9	5729.4	4435.5	2911.3	1675.7	947.7

ADC sampling rate = 256kHz										
OSR			128	256	512	1024	2048	4096	8192	16384
Gain	200	**ENOB**	13.6	14.2	14.7	15.2	15.7	16.1	16.5	17.0
		Vn_{rms}(nV)	451.6	322.6	231.3	163.9	117.2	83	64.2	46.7
	100	**ENOB**	14.6	15.1	15.6	16	16.5	16.9	17.4	17.9
		Vn_{rms}(nV)	478.7	341.1	245.2	182.4	132.7	96	67.8	49.4
	1	**ENOB**	16.2	16.7	16.9	17.2	17.5	18.4	19.4	20.2
		Vn_{rms}(nV)	15634	11431.5	9730	8411.7	6766	3991.1	1772.2	1010.1

Remark:

The above data are averages based on multiple ICs' measured results. Each IC contributes 1024 data points.

ENOB = $\log_2(\frac{FRS}{Vrms})$, FRS is the Full Scale Voltage Range (2 * Vref / Gain), Vrms is the rms Noise.

Oscillator Characteristics

Figure 4 and figure 5 are SD8304 oscillating frequency as function of power supply voltage from five parts.

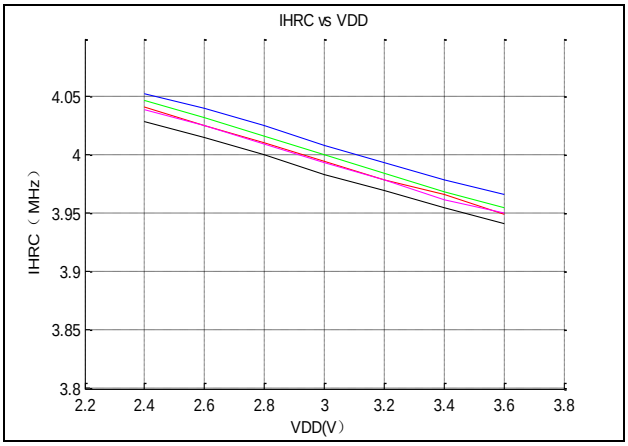


Figure 4. IHRC frequency vs voltage

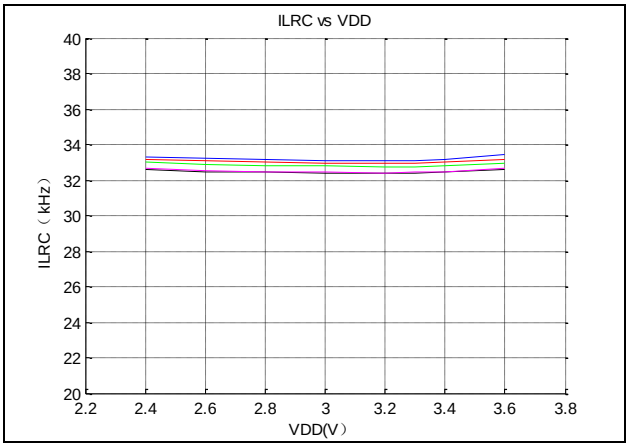


Figure 5. ILRC frequency vs voltage

Figure 6 and figure 7 are SD8304 oscillating frequency as function of temperature from five parts.

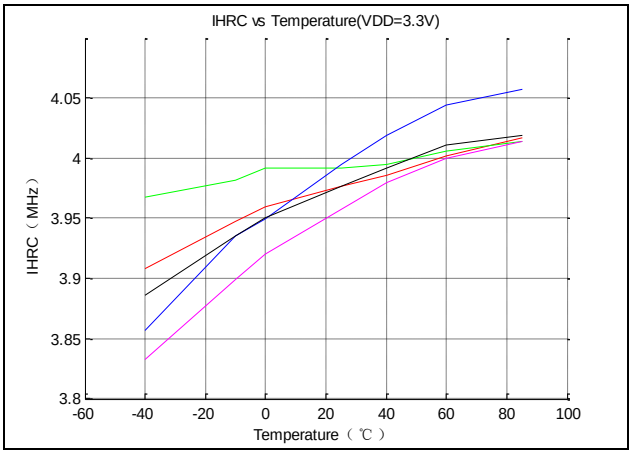


Figure 6. IHRC frequency vs temperature

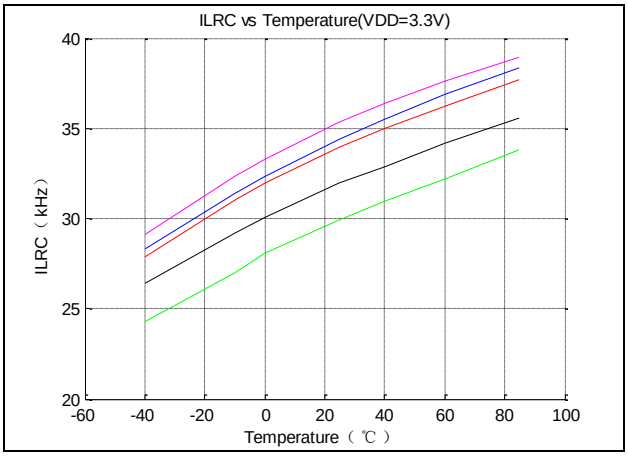


Figure 7. ILRC frequency vs temperature

Electrical Specification

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
T_A	Operating temperature	-40	+85	℃
T_S	Storage temperature	-55	+150	℃
V_{DD}	Supply voltage	-0.2	+4.0	V
Vpp	Programming voltage	-0.2	+7.5	V
V_{IN}, V_{OUT}	Digital input/output voltage	-0.2	V_{DD}+0.3	V
T_L	Reflow temperature profile	Per IPC/JEDECJ-STD-020C		℃

Remarks:
1. CMOS device can easily be damaged by electrostatics. It must be stored in conductive foam, and careful not to exceed the operating voltage range.
2. Turn off power before insert or remove the device.

Table 4. Electrical Specifications (VDD=3V, T_A=25 ˚C)

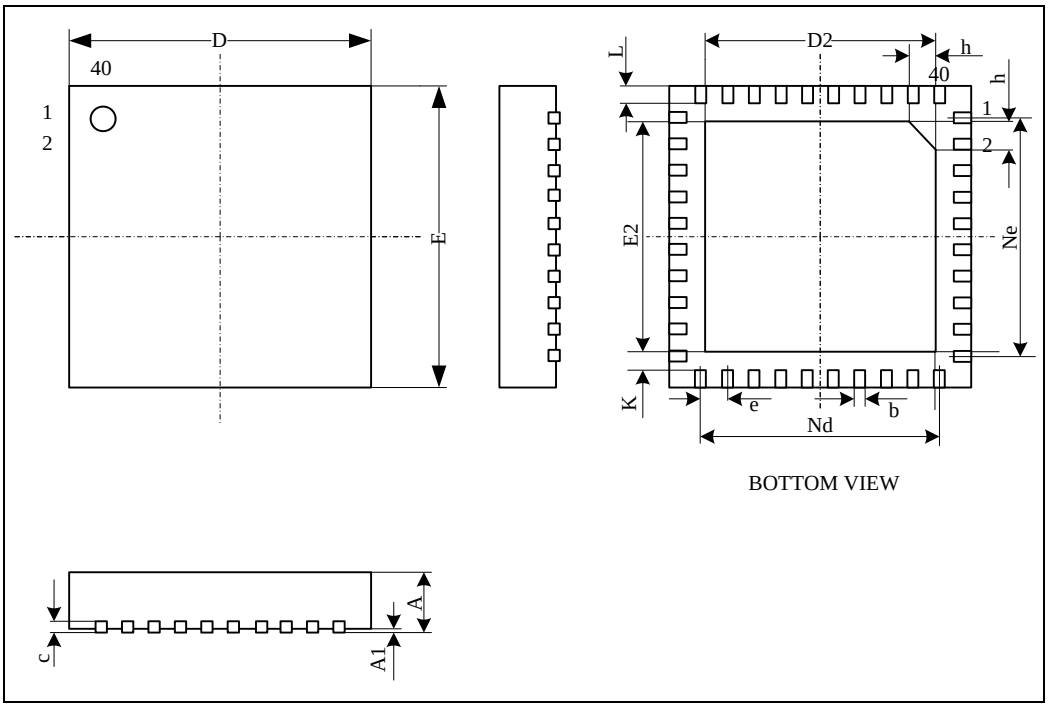
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Remarks
VDD	Supply voltage	2.4	3.0	3.6	V	Analog modules operating voltage
		2.0	3.0	3.6	V	Digital modules and MCU operating voltage
FOSC	Operating frequency	0.016	2	4	MHz	FOSC must be 2MHz when read/write tables in OTP
IHRC	Internal high frequency RC oscillator	--	4	--	MHz	Frequency after calibration
ILRC	Internal low frequency RC oscillator	28	--	36	kHz	Frequency after calibration
LXT	External low frequency crystal oscillator	16	32.768	100	kHz	
IDD1	Operating current 1	--	800	--	uA	4MHz internal RC oscillator freq halved for MCU Digital and analog modules both active
IDD2	Operating current 2	--	6	--	uA	32kHz internal RC oscillator for MCU Digital modules active Analog modules inactive
IDD3	Operating current 3	--	1	--	uA	32kHz internal RC oscillator for MCU MCU at standby mode Analog modules inactive
IDD4	Operating current 4	--	--	1	uA	MCU at sleep mode Analog modules inactive
Fsam	ADC sampling rate	--	--	256	kHz	
OSR	Over sampling rate	128	--	16384		
NFbit	Noise free bits[1]	--	16	--	bits	Gain=200, input FSR= ±4mV
VINpga	PGIA differential input range[2]	-Vref	--	Vref	mV	1X gain
		-Vref/12.5	--	Vref/12.5		12.5X gain
		-Vref/50	--	Vref/50		50X gain
		-Vref/100	--	Vref/100		100 X gain
		-Vref/200	--	Vref/200		200 X gain

Vavddr	AVDDR Voltage output	--	2.4	--	V	AVDDRX [1:0]=00
		--	2.6	--		AVDDRX [1:0]=01
		--	2.9	--		AVDDRX [1:0]=10
		--	3.3	--		AVDDRX [1:0]=11
Iavddr	AVDDR current	--	10	--	mA	
POR	POR voltage	--	2.0	--	V	
LVD	LVD voltage	--	1.9	--	V	
THlbt	LVD hysteresis	--	200	--	mV	
Vlbt	Low VDD alarm threshold	--	--	--	V	LBTX[3:0]=0000~0111 : Vlbt OFF
		--	LBTIN	--		LBTX[3:0]=1000
		--	3.05	--		LBTX[3:0]=1001
		--	2.95	--		LBTX[3:0]=1010
		--	2.85	--		LBTX[3:0]=1011
		--	2.75	--		LBTX[3:0]=1100
		--	2.65	--		LBTX[3:0]=1101
		--	2.55	--		LBTX[3:0]=1110
		--	2.45	--		LBTX[3:0]=1111
Vlcd	LCD charge pump output voltage	--	2.3	--	V	VLCDX[1:0]=00
		--	2.5	--		VLCDX[1:0]=01
		--	2.7	--		VLCDX[1:0]=10
		--	2.9	--		VLCDX[1:0]=11
Ilcd	LCD charge pump current[3]	--	--	500	uA	connect 1uF capacitor to VDD
Digital I/O parameter						
IOH	Output high current source	--	12	--	mA	VOH=VDD-0.3V
IOL	Output low current sink	--	12	--	mA	VOL=0.3V
VIH	Input high voltage	0.7VDD	--	--	V	
VIL	Input low voltage	--	--	0.3VDD	V	
VOH	Output high voltage	VDD-0.3	--	--	V	
VOL	Output low voltage	--	--	VSS+0.3	V	
Rpu	Pin pull up resistance	--	50	--	kΩ	VDD = 3.0

Note:

1. Noise free bits and effective resolution are both related to the signal's full scale range. Its peak to peak or rms noise plays the decisive role.
2. The signal input range is limited by the differential signal input range and the absolute voltage at the input terminals. The first one is the real signal input range. It is affected by the PGIA gain and the ADC voltage reference choice. The second one includes both differential and common mode components and is mainly limited by the circuit.
3. The charge pump driving capability is related to the choice of capacitor and the operating frequency.

Packaging Information



Dimensions: mm

Symbol	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	——	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.30	3.40	3.50
e	0.40BSC		
Nd	3.60BSC		
E	4.90	5.00	5.10
E2	3.30	3.40	3.50
Ne	3.6BSC		
L	0.30	0.35	0.40
K	0.20	——	——
h	0.30	0.35	0.40

Figure 8. QFN40 mechanical specification