SD8118

4 Diff Channels ADC SOC with 8 Bits DAC and 24*4 LCD

Features

- High precision ADC, ENOB=18.7bits@8sps, 4 differential or 8 single-ended inputs
- Low noise, high input impedance preamplifier with selectable gain: 1, 4, 8, 16, 32, 64, 128, or 256
- 8 bits RISC ultra-low power MCU, 49 instructions and 6 stack levels. The MCU current consumption is 400uA typically at 3V and 2MHz operating clock rate. Standby current is 1.5uA at 32kHz clock, and less than 1uA at sleep
- 16K Bytes OTP, 512 Bytes SRAM
- Low OTP programming voltage, can replace external EEPROM
- Flexible battery voltage detection range 2.0V~ 3.3V
- RTC module provides calendar/time information, automatic leap year calculation
- Abundant peripheral resources: UART, PWM, PDM, PFD, TIMER, infrared carrier generator, sine wave generator
- 24SEG X 4COM, 23SEG X 5COM, 22SEG X 6COM, 20SEG X 8COM LCD drive, ultra-low power consumption and high driving capability, programmable boost module to maintain luminance at low supply voltage
- 8bits DAC
- Every digital I/O port contain Schmitt trigger input and selectable pull up resistor
- Low voltage detection and power on reset circuit
- Operating voltage range: 2.4V~ 3.6V
- Operating temperature range: -40 ˚C~85 ˚C
- Built-in 8MHz and 32kHz RC oscillators

Description

The SD8118 is a CMOS SOC with built-in 24 bit ADC and 16k Bytes OTP memory.

The IC was designed with ultra-low power technology. Operates at 3V supply and quarter internal RC oscillator frequency, the total typical operating current is 1.5mA.

It has very rich peripheral resources: RTC, UART, selectable regulated voltage source, flexible PGIA setup, voltage booster, TIMER, PWM, PFD, and LCD driver.

The OTP can be programmed in situ and the 2.4V~3.6V programming voltage is generated internally. The OTP can be used in place of external EEPROM.

Three working modes are provided so users can select the optimum choice between speed and power. They are normal mode, standby mode, and sleep mode.

Applications

Four electrodes AC health scale, cash register scale, infrared temperature measurement,

Ordering Information

SSOP48 package

Pin Diagram and Descriptions

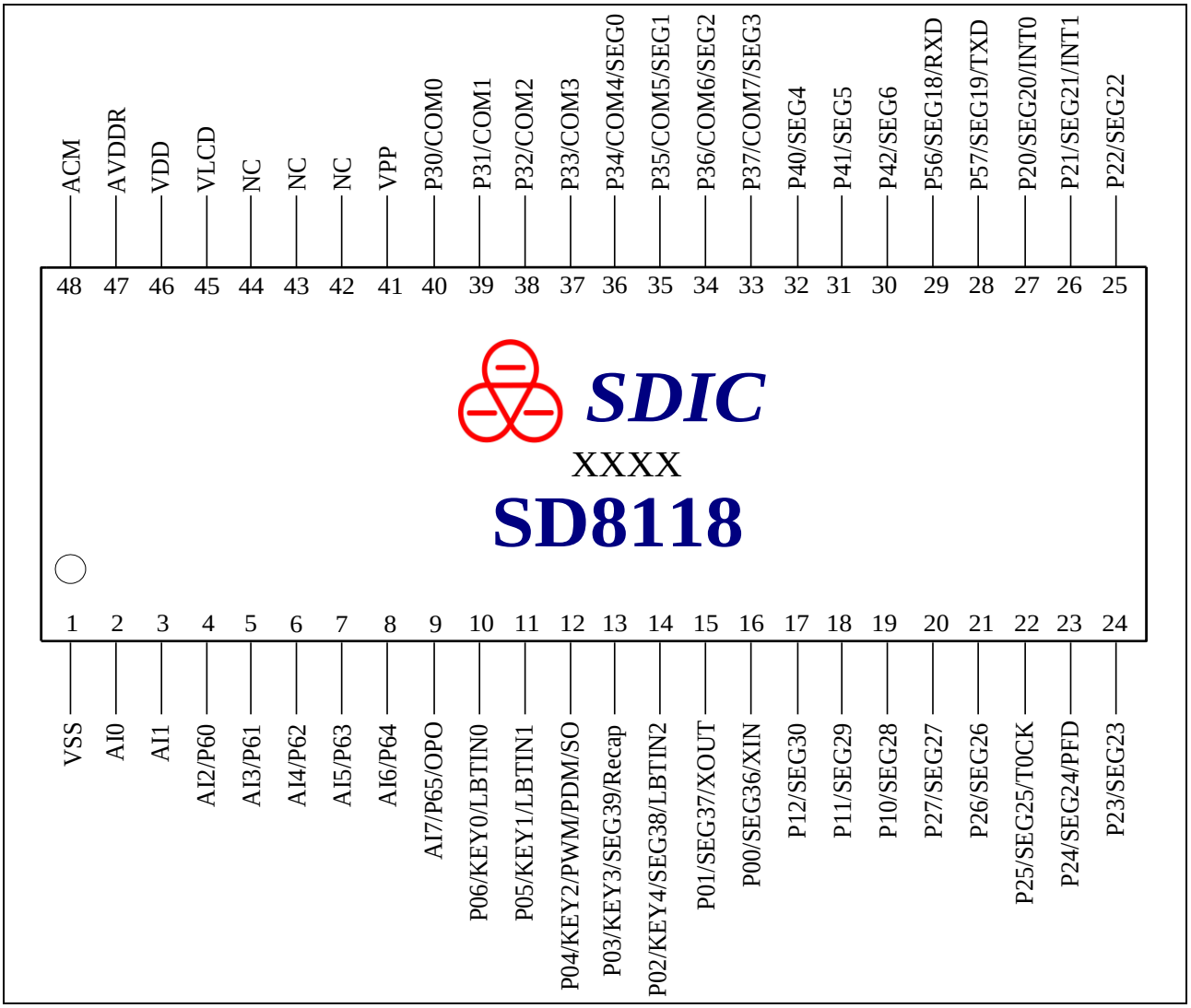


Figure 1. Pad diagram

Table 1. Pad Descriptions

Pad No.	Pin Name	Attribute	Description
1	VSS	Ground	Power ground
2-3	AI0 – AI1	Analog input	Analog signal inputs, each port has an independent register controlled pull-down resistor (default OFF), should set to ON for unused port; Can be used as one differential or two single-ended inputs
4-9	AI2/P60-- AI7/P65/OPO	Analog, I/O	AI2-7 are analog signal inputs. AI2-3, AI4-5, AI6-7 can be used as 3 differential or 6 single-ended inputs, or digital port P60-65. Pin 9 can be used as amplifier OPA's output OPO
10	P06/KEY0/LBTIN0	Analog, I/O	Digital port P06, external key interrupt input KEY0, or low battery detect LBTIN0 input
11	P05/KEY1/LBTIN1	Analog, I/O	Digital port P05, external key interrupt input KEY1, or low battery detect LBTIN1 input
12	P04/KEY2/ PWM/PDM/SO	I/O	Digital port P04, external key interrupt input KEY2, PWM/PDM output, or 5k/50k/100kHz sine wave output SO
13	P03/KEY3/SEG39/ Recap	Analog, I/O	Digital port P03, external key interrupt input KEY3, LCD segment SEG39, or amplifier OPB's output Recap
14	P02/KEY4/SEG38/ LBTIN2	Analog, I/O	Digital port P02, external key interrupt input KEY4, LCD segment SEG38, or low battery detect LBTIN2 input
15-16	P01/SEG37/XOUT-- P00/SEG36/XIN	Analog, I/O	Digital ports P01-00, LCD segment SEG37-36, or 32.768kHz or 1-8MHz crystal oscillator pins. XIN can be used as external clock input
17-19	P12/SEG30-- P10/SEG28	I/O	Digital ports P12-10 or LCD segment SEG30-28
20-21	P27/SEG27-- P26/SEG26	I/O	Digital ports P27-26 or LCD segment SEG27-26
22	P25/SEG25/T0CK	I/O	Digital port P25, LCD segment SEG25, or TIMER0 external clock input T0CK
23	P24/SEG24/PFD	I/O	Digital port P24, LCD segment SEG24, or Programmable frequency divider PFD output
24-25	P23/SEG23-- P22/SEG22	I/O	Digital ports P23-22 or LCD segment SEG23-22
26	P21/SEG21/INT1	I/O	Digital port P21, LCD segment SEG21, or external interrupt INT1
27	P20/SEG20/INT0	I/O	Digital port P20, LCD segment SEG20, or external interrupt INT0
28	P57/SEG19/TXD	I/O	Digital port P57, LCD segment SEG19, or UART data transmit TXD
29	P56/SEG18/RXD	I/O	Digital port P56, LCD segment SEG18, or UART data receive RXD
30-32	P42/SEG6 -- P40/SEG4	I/O	Digital port P42-40 or LCD segment SEG6-4
33-36	P37/COM7/SEG3-- P34/COM4/SEG0	I/O	Digital port P37-34, LCD COM7-4, or COM3-0 at 4COM mode
37-40	P33/COM3-- P30/COM0	I/O	Digital port P33-30 or LCD COM3-0 During serial programming, Pin 37-40 serve as Data output, 2MHz clock input, Data input, and Data clock
41	VPP	I	OTP high voltage programming pin, connect 1uF capacitor to VSS
42-44	NC	NC	Leave floating, do not connect to any circuit
45	VLCD	Analog	LCD driver power supply, internally connect to VDD or booster output through register setting, connect 1uF filter capacitor to VDD

46	VDD	Power	Power supply voltage, connect 0.1uF capacitor to VSS
47	AVDDR	Analog	Internal LDO output for IC's analog module, can provide excitation to external transducer, connect 0.1uF to 10uF filter capacitor to VSS
48	ACM	Analog	1.2V reference output, floating when ACM is shutdown, connect 0.1uF cap to VSS

Remark: All I/O ports Pnn have internal pull-up option (default OFF) and input hysteresis at 0.3VDD/0.7VDD.

Functional Block

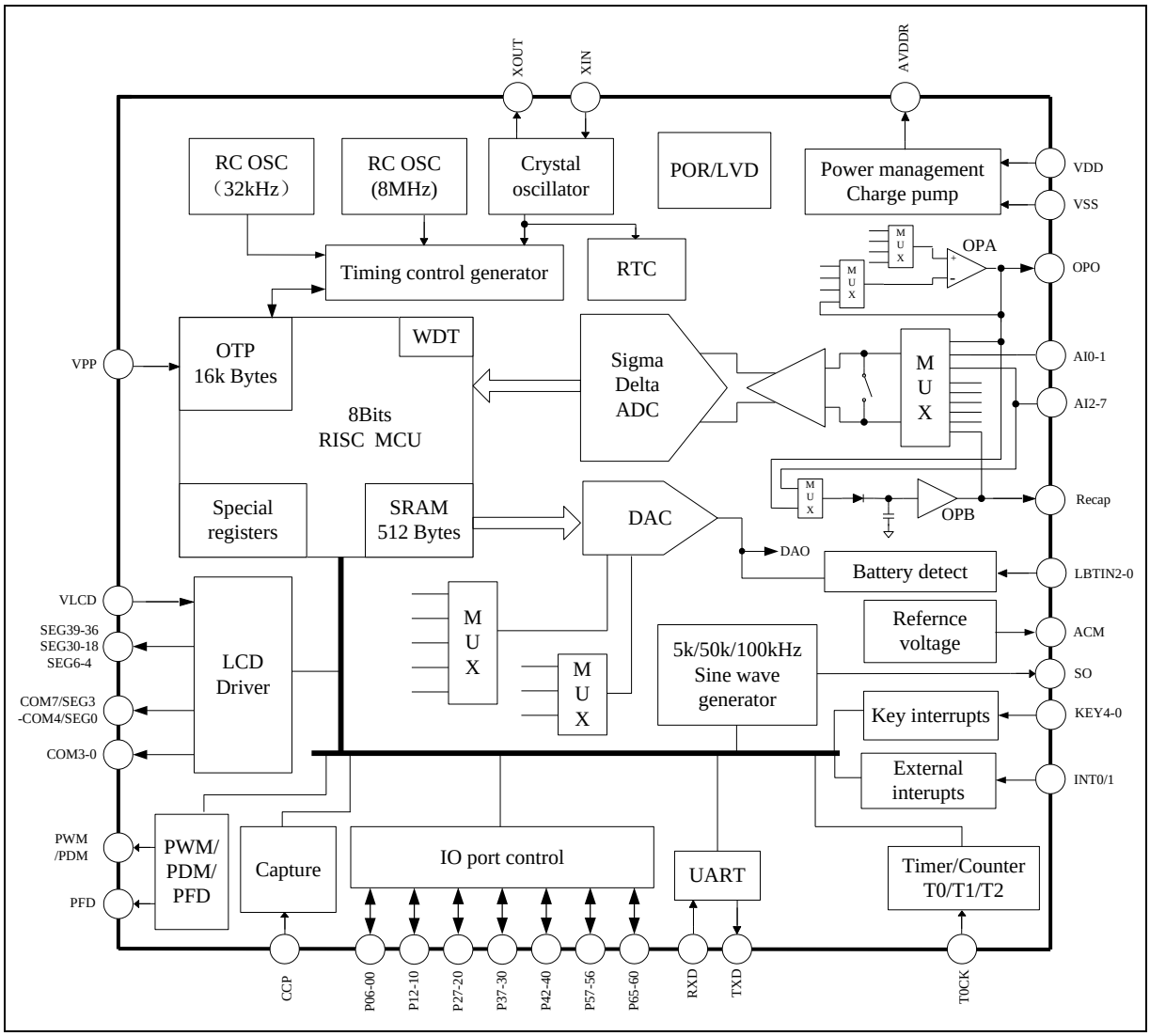


Figure 2. Functional block diagram

Typical Applications

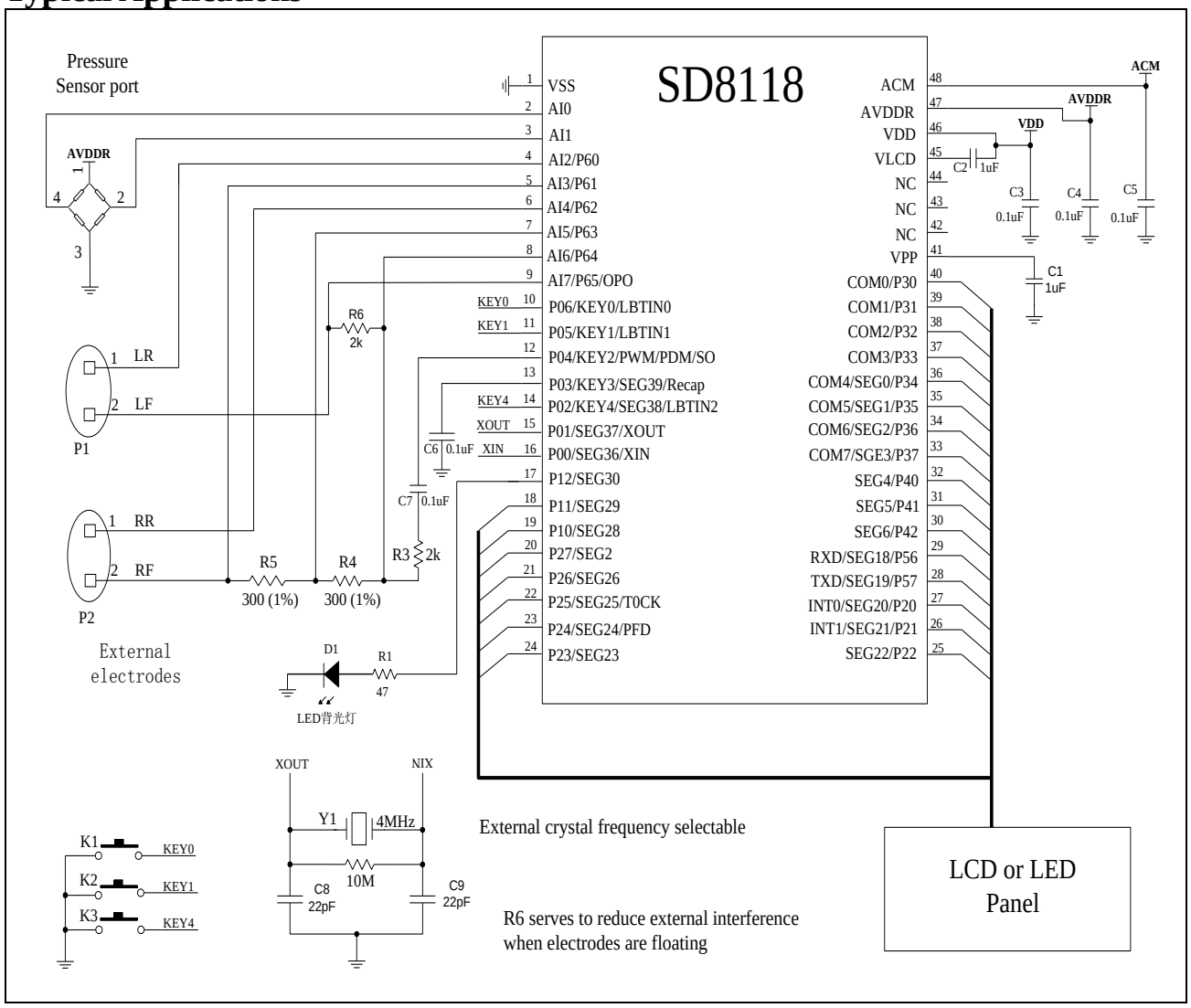


Figure 3. Four electrodes AC health scale

ADC Characteristics

Table 2. ENOB and voltage noise Vn_{rms} (AVDDR=2.4V, VREF=0.6V, SINC3, Buffer on)

ADC sampling rate = 128kHz										
OSR			128	256	512	1024	2048	4096	8192	16384
Gain	256	**ENOB**	14.1	14.6	15.1	15.6	16.1	16.6	17.0	17.5
		Vn_{rms}(nV)	262	185	132	93	66	47	35	26
	128	**ENOB**	15.0	15.6	16.0	16.6	17.0	17.6	18.1	18.7
		Vn_{rms}(nV)	277	195	138	98	69	49	32	22
	1	**ENOB**	16.8	17.4	17.9	18.4	18.9	19.4	19.9	20.3
		Vn_{rms}(nV)	10868	6880	4846	3405	2372	1681	1217	901

ADC sampling rate = 512kHz										
OSR			128	256	512	1024	2048	4096	8192	16384
Gain	256	**ENOB**	13.2	13.7	14.2	14.7	15.2	15.7	16.3	16.7
		Vn_{rms}(nV)	486	344	242	171	124	90	60	43
	128	**ENOB**	14.2	14.7	15.2	15.8	16.3	16.8	17.3	17.8
		Vn_{rms}(nV)	498	352	245	170	120	84	59	42
	1	**ENOB**	16.8	17.4	17.8	18.1	18.5	19.2	19.9	20.4
		Vn_{rms}(nV)	10880	7162	5374	4171	3153	2011	1220	897

Remark:

The above data are averages based on multiple ICs' measured results. Each IC contributes 1024 data points.

ENOB = $\log_2(\frac{FRS}{Vrms})$, FRS is the Full Scale Voltage Range (2 * Vref / Gain), Vrms is the rms Noise.

Electrical Specifications

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
T_A	Operating temperature	-40	+85	℃
T_S	Storage temperature	-55	+150	℃
V_{DD}	Supply voltage	-0.2	+4.0	V
Vpp	Programming voltage	-0.2	+7.5	V
V_{IN}, V_{OUT}	Digital input/output voltage	-0.2	V_{DD}+0.3	V
T_L	Reflow temperature profile	Per IPC/JEDECJ-STD-020C		℃

Remarks:

1. CMOS device can easily be damaged by electrostatics. It must be stored in conductive foam, and careful not to exceed the operating voltage range.
2. Turn off power before insert or remove the device.

Table 4. Electrical Specifications（VDD=3V, T_A=25℃）

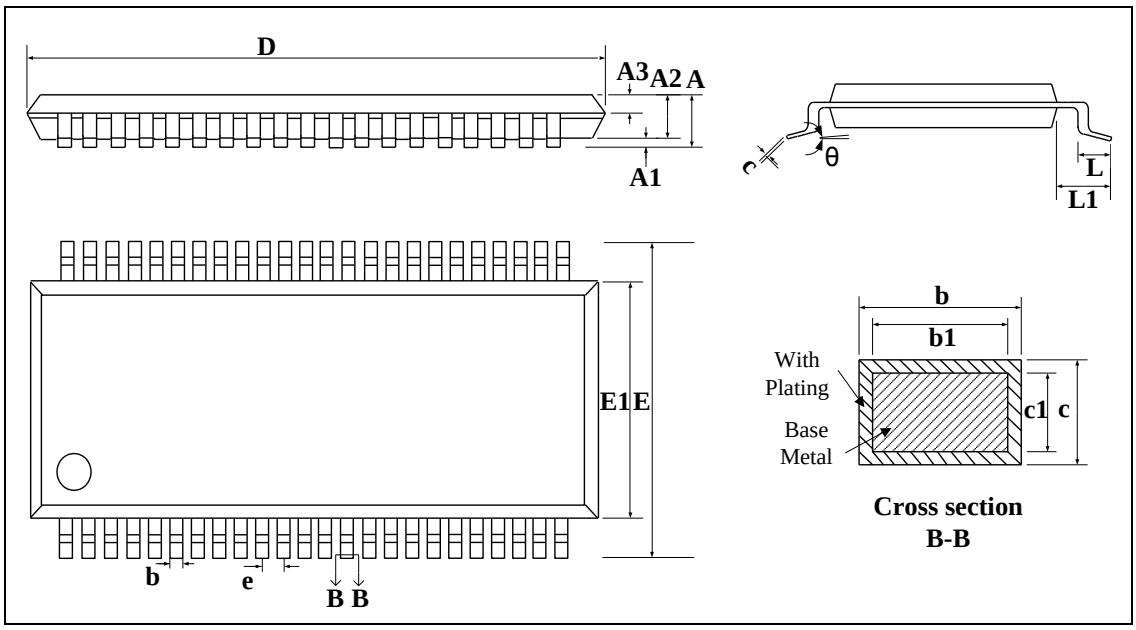
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Remarks
VDD	Supply voltage	2.4	3.0	3.6	V	Analog modules operating voltage
		2.0	3.0	3.6	V	Digital modules and MCU operating voltage
FOSC	Operating frequency	0.016	2	4	MHz	FOSC must be 2MHz when read/write tables in OTP
IHRC	Internal high frequency RC oscillator	--	8	--	MHz	Frequency after calibration
ILRC	Internal low frequency RC oscillator	28	--	36	kHz	Frequency after calibration
HXT	External high frequency crystal oscillator	1	--	4	MHz	
LXT	External low frequency crystal oscillator	16	32.786	--	kHz	
IDD1	Operating current 1	--	1.5	--	mA	Internal RC oscillator freq quartered for MCU Analog modules active
IDD2	Operating current 2	--	2	--	uA	32kHz internal RC oscillator for MCU MCU at standby mode Analog modules inactive
IDD3	Operating current 3	--	1	--	uA	MCU at sleep mode Analog modules inactive
Fsam	ADC sampling rate	--	--	512	kHz	
OSR	Over sampling rate	128	--	16384		
NFbit	Noise free bits[1]	--	16	--	bits	Gain=128, input FSR=±4mV
NMbit	No missing code	--	--	24	bits	
INL	INL	--	0.002	--	%FSR	
VINdif	PGIA differential input range	-Vref	--	Vref	mV	1X gain
		-Vref/4	--	Vref/4		4X gain
		-Vref/8	--	Vref/8		8X gain
		-Vref/16	--	Vref/16		16X gain
		-Vref/32	--	Vref/32		32X gain
		-Vref/64	--	Vref/64		64X gain

		-Vref/128	--	Vref/128		128X gain
		-Vref/256	--	Vref/256		256X gain
VIN	PGIA input voltage range[2]	-0.3	--	AVDDR		1X gain and buffer is off
		0.3	--	AVDDR-0.7		1X gain and buffer is on, or gain≠1
Vnrms	RMS noise	--	26	--	nVrms	256X gain
Vacm	ACM voltage output	--	1.2	--	V	
IacmSour	ACM current source	--	1	--	mA	
IacmSink	ACM current sink	--	1	--	mA	
PSRacm	ACM PSR	--	100	--	uV/V	
Tgain	Gain tempco	--	±4	--	ppm/℃	-10℃ to +40℃
Vavddr	AVDDR voltage output	--	2.4	--	V	AVDDRX [1:0]=00
		--	2.6	--		AVDDRX [1:0]=01
		--	2.9	--		AVDDRX [1:0]=10
		--	3.3	--		AVDDRX [1:0]=11
Iavddr	AVDDR current	--	10	--	mA	
POR	POR voltage	--	2.0	--	V	
LVD	LVD voltage	--	1.9	--	V	
THlbt	LVD hysteresis	--	200	--	mV	
Vlcd	LCD charge pump output voltage	--	2.5	--	V	VLCDX[2:0]=000
		--	2.7	--		VLCDX[2:0]=001
		--	2.9	--		VLCDX[2:0]=010
		--	3.1	--		VLCDX[2:0]=011
		--	3.2	--		VLCDX[2:0]=100
		--	3.3	--		VLCDX[2:0]=101
		--	3.5	--		VLCDX[2:0]=110
		--	3.6	--		VLCDX[2:0]=111
Ilcd	LCD charge pump current[3]	--	--	500	uA	
Digital I/O parameter						
IOH	High output current source	--	3	--	mA	VOH=VDD-0.3V, PTxSR=0
		--	12	--		VOH=VDD-0.3V, PTxSR=1
IOL	Output low current sink	--	3	--	mA	VOL=0.3V, PTxSR=0
		--	12	--		VOL=0.3V, PTxSR=1
VIH	Input high voltage	0.7VDD	--	--	V	
VIL	Input low voltage	--	--	0.3VDD	V	
VOH	Output high voltage	VDD-0.3	--	--	V	
VOL	Output low voltage	--	--	VSS+0.3	V	
Rpu	Pin pull up resistance	--	50	--	kΩ	VDD = 3.0

Note:

1. Noise free bits and effective resolution are both related to the signal's full scale range. Its peak to peak or rms noise plays the decisive role.
2. The signal input range is limited by the differential signal input range and the absolute voltage at the input terminals. The first one is the real signal input range. It is affected by the PGIA gain and the ADC voltage reference choice. The second one includes both differential and common mode components and is mainly limited by the circuit.
3. The charge pump driving capability is related to the choice of capacitor and the operating frequency.

Packaging Information



Dimensions:mm

Symbol	Min.	Nom.	Max.
A	——	——	2.80
A1	0.20	0.30	0.40
A2	2.20	2.30	2.40
A3	1.02	1.07	1.12
b	0.24	0.25	0.28
c	0.14	——	0.23
D	15.80	15.90	16.00
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	0.635BSC		
L	0.61	——	0.91
L1	1.40REF		
θ	0	——	8

Figure 4. SSOP48 mechanical specification