SD8111
Meterage SOC

Features（latest 0.1c）

- High precision 24 bits ADC, 18 bits effective resolution, 1 differential or 2 single-ended inputs
- Low noise, high input impedance preamplifier with selectable gain: 1, 12.5, 50, 100, or 200; 90nVrms equivalent input noise at 200X gain and 8SPS output rate
- 8 bits RISC ultra low power MCU. At 2MHz operating clock rate and 3V, current consumption is 300uA typically, 1.5uA at standby and 32kHz clock, and less than 1uA at sleep
- 16k Bytes OTP, 256 Bytes SRAM
- Support external 32.768kHz or similar oscillator
- Real time clock provides second, minute, hour data
- ADC output rate: 8SPS-2kSPS
- 14SEG X 4COM LCD drive, LED drivers
- Built-in temperature sensor, supports single point calibration
- Selectable voltage source: 2.4V/2.6V/2.9V/3.3V
- Flexible battery voltage detection: 2.0V~ 3.3V
- Low voltage detection and power on reset circuit
- Operating voltage range: 2.4V~ 3.6V
- Operating temperature range: -40℃~ 85℃

Description

The SD8111 is a CMOS SOC with built-in 24 bits ADC and low programming voltage OTP memory. LCD ports can drive LED too. The OTP can be used for software calibration.

The IC was designed with ultra low power technology. Operating at 2MHz clock rate and 3V supply, the MCU itself only consumes 300uA. With ADC active, the total typical operating current is 750uA. Such low current consumption is very suitable for battery powered applications.

The IC has strong anti-interference capability. It passes 4kV Electrical Fast Transient (EFT) test easily without using any additional protective circuit, and is suitable for harsh environment applications.

Applications

Measuring instrument

Ordering Information

LQFP48 package

Pin Diagram and Descriptions

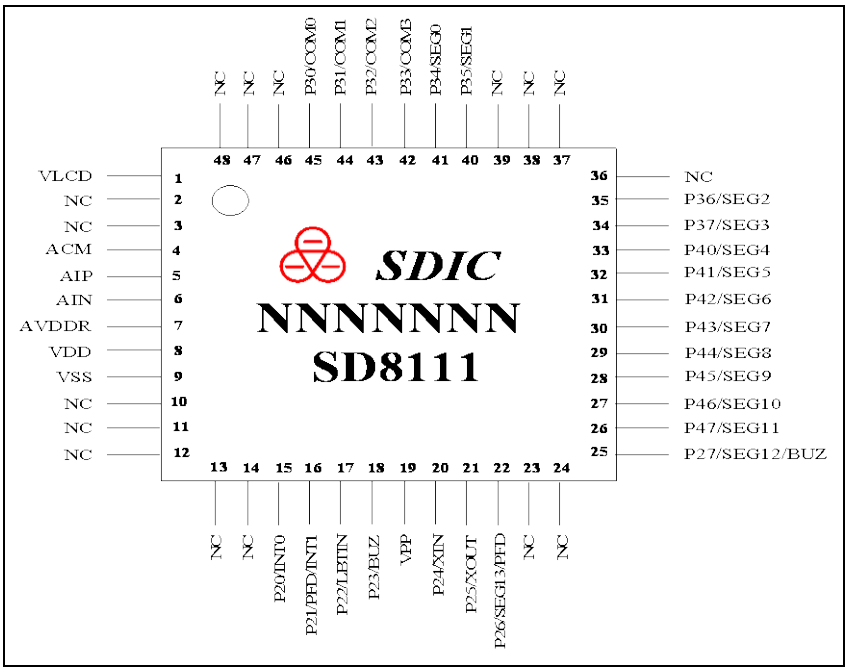


Figure 1. Pad diagram

Table 1. Pad Descriptions

Pad No.	Pin Name	Attribute	Description
1	VLCD	Analog	LCD driver power supply, internally connect to VDD or booster output through register setting, connect 1uF filter capacitor to VDD
2-3	NC	--	No connect. Float, or short to VDD or VSS
4	ACM	Analog	1.2V reference output, floating when ACM is shutdown, connect 0.1uF cap to VSS
5	AIP	Analog input	Analog signal differential or two single-ended inputs Should enable the internal pull-down resistor for unused input
6	AIN		
7	AVDDR	Analog	Internal LDO output for IC's analog module, can provide excitation to external transducer, connect 0.1uF filter capacitor to VSS
8	VDD	Power	Power supply voltage, connect 0.1uF capacitor to VSS
9	VSS	Ground	Ground
10-14	NC	--	No connect. Float, or short to VDD or VSS
15	P20/INT0	I/O	Digital port P20 or external interrupt INT0
16	P21/PFD/INT1	I/O	Digital port P21, programmable frequency divider PFD output, or external interrupt INT1
17	P22/LBTIN	I/O	Digital port P22 or low battery detect LBTIN input
18	P23 /BUZ	I/O	Digital port P23 or buzzer BUZ output
19	VPP	I	OTP high voltage programming pin, connect 1uF capacitor to VDD or VSS
20	P24/XIN	I/O	Digital port P24 or low frequency crystal oscillator input XIN
21	P25 /XOUT	I/O	Digital port P25 or low frequency crystal oscillator output XOUT
22	P26/SEG13 /PFD	I/O	Digital port P26, LCD segment SEG13, or Programmable Frequency Divider PFD
23-24	NC	--	No connect. Float, or short to VDD or VSS
25	P27/SEG12 /BUZ	I/O	Digital port P27, LCD segment SEG12, or BUZ output
26-35	P47/SEG11 -- P36/SEG2	I/O	Digital port P47-40/P37-36, or LCD SEG11-2
36-39	NC	--	No connect. Float, or short to VDD or VSS
40	P35/SEG1	I/O	Digital port P35 or LCD SEG1
41	P34/SEG0	I/O	Digital port P34 or LCD SEG0
42-45	P33/COM3-- P30/COM0	I/O	Digital port P33-30 or LCD COM3-0
46-48	NC	--	No connect. Float, or short to VDD or VSS

Remark: All I/O ports Pnn have internal pull-up option (default OFF) and input hysteresis at 0.3VDD/0.7VDD.

Functional Block

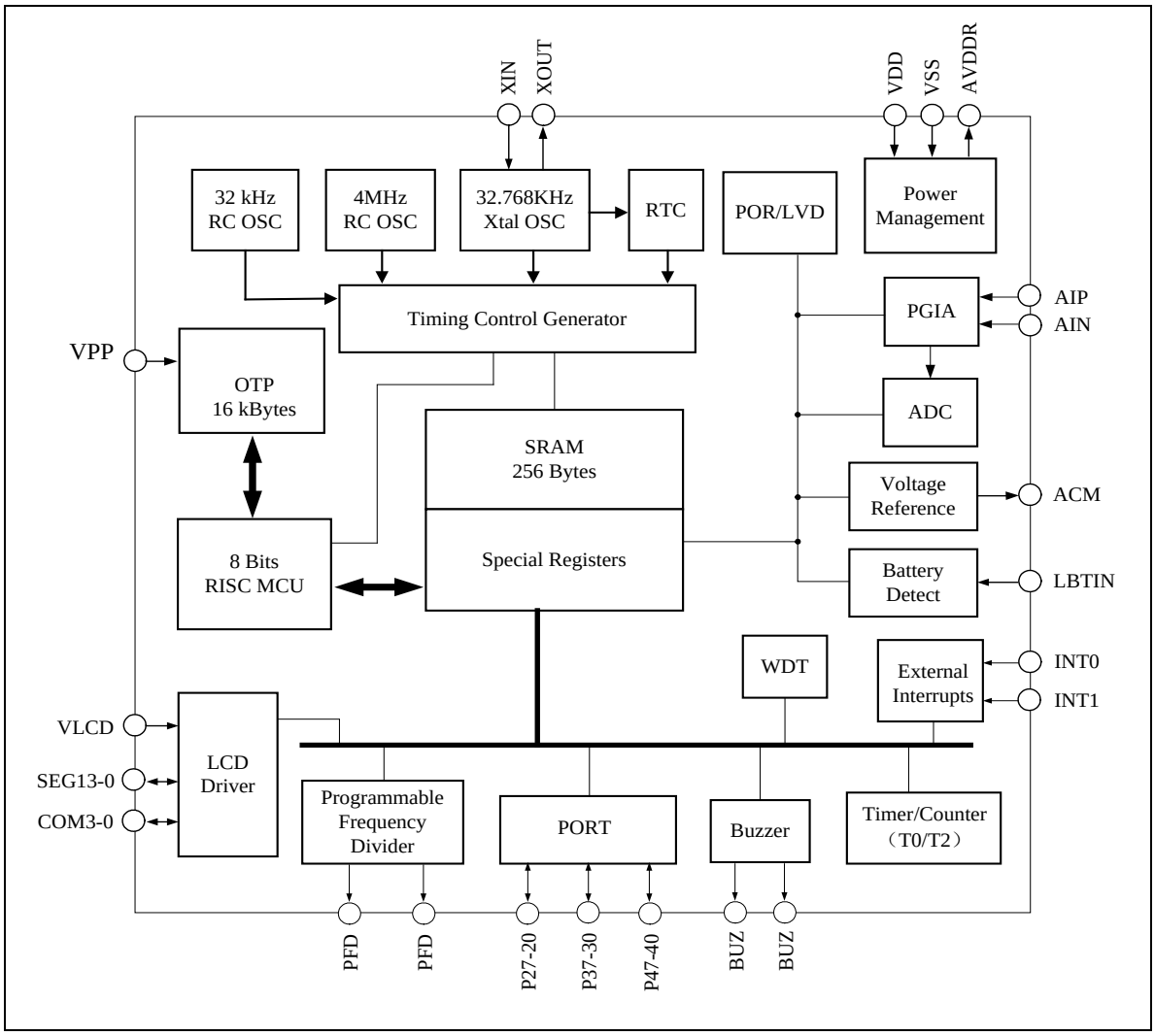


Figure 2. Functional block diagram

Typical Applications

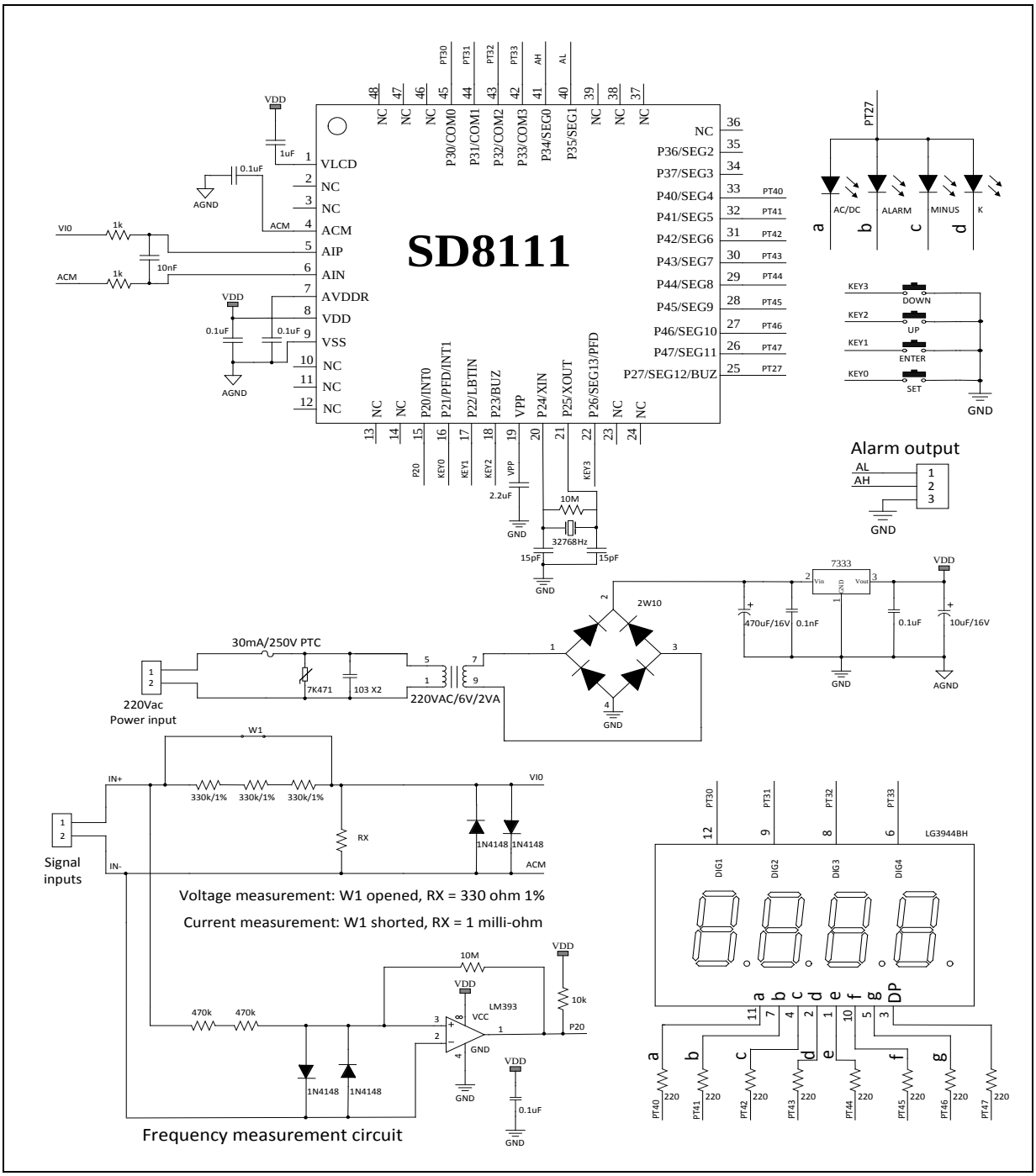


Figure 3. Voltage meter/Current meter typical application diagram

Electrical Specifications

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
T_A	Operating temperature	-40	+85	℃
T_S	Storage temperature	-55	+150	℃
V_{DD}	Supply voltage	-0.2	+4.0	V
Vpp	Programming voltage	-0.2	+7.5	V
V_{IN}, V_{OUT}	Digital input/output voltage	-0.2	V_{DD}+0.3	V
T_L	Reflow temperature profile	Per IPC/JEDECJ-STD-020C		℃

Remarks:

1. CMOS device can easily be damaged by electrostatics. It must be stored in conductive foam, and careful not to exceed the operating voltage range.
2. Turn off power before insert or remove the device.

Table 3. Electrical Specifications（VDD=3V, T_A=25℃）

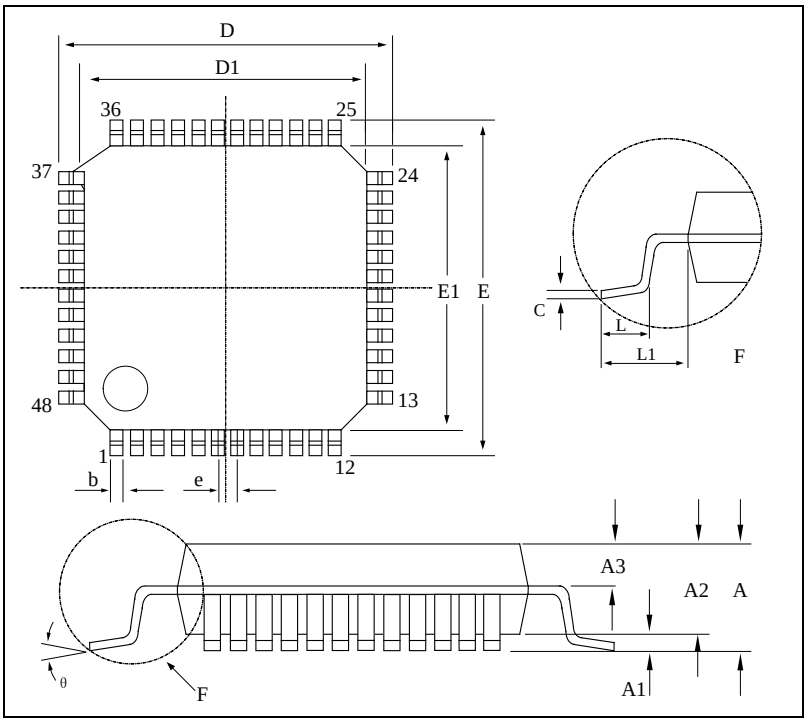
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Remarks
VDD	Supply voltage	2.4	3.0	3.6	V	Analog modules operating voltage
		2.0	3.0	3.6	V	Digital modules and MCU operating voltage
FOSC	Operating frequency	16k	2M	4M	Hz	FOSC must be 2MHz when read/write tables in OTP
IHRC	Internal high frequency RC oscillator	3.9	--	4.1	MHz	Frequency after calibration
ILRC	Internal low frequency RC oscillator	28	--	36	kHz	Frequency after calibration
LXT	External low frequency crystal oscillator	16	32.786	--	kHz	
IDD1	Operating current 1	--	750	--	uA	2MHz internal RC oscillator for MCU Analog and digital modules active
IDD2	Operating current 2	--	6	--	uA	32kHz internal RC oscillator for MCU Digital modules active Analog modules inactive
IDD3	Operating current 3	--	1	--	uA	32kHz internal RC oscillator for MCU MCU at standby mode Analog modules inactive
IDD4	Operating current 4	--	0.2	1	uA	MCU at sleep mode Analog modules inactive
Fsam	ADC sampling rate	--	128	256	kHz	
OSR	Over sampling rate	128	--	16384		
NFbit	Noise free bits[1]	--	16	--	bits	Gain=1，input FSR=±800mV
VINdif	PGIA differential input range	--	--	1800	mV	1X gain
		-Vref/12.5	--	Vref/12.5		12.5X gain
		-Vref/50	--	Vref/50		50X gain
		-Vref/100	--	Vref/100		100 X gain
		-Vref/200	--	Vref/200		200 X gain

Vavddr	AVDDR Voltage output	--	2.4	--	V	AVDDRX [1:0]=00
		--	2.6	--		AVDDRX [1:0]=01
		--	2.9	--		AVDDRX [1:0]=10
		--	3.3	--		AVDDRX [1:0]=11
Iavddr	AVDDR current	--	10	--	mA	
POR	POR voltage	--	2.0	--	V	
LVD	Low Voltage Detect reset voltage	--	1.9	--	V	
THlbt	LVD hysteresis	--	200	--	mV	
Vlbt	Low VDD alarm threshold	--	3.3	--	V	LBTX[3:0]=0010
		--	3.2	--		LBTX[3:0]=0011
		--	3.1	--		LBTX[3:0]=0100
		--	3.0	--		LBTX[3:0]=0101
		--	2.9	--		LBTX[3:0]=0110
		--	2.8	--		LBTX[3:0]=0111
		--	2.7	--		LBTX[3:0]=1000
		--	2.6	--		LBTX[3:0]=1001
		--	2.5	--		LBTX[3:0]=1010
		--	2.4	--		LBTX[3:0]=1011
		--	2.3	--		LBTX[3:0]=1100
		--	2.2	--		LBTX[3:0]=1101
		--	2.1	--		LBTX[3:0]=1110
		--	2.0	--		LBTX[3:0]=1111
Vlcd	LCD charge pump output voltage	--	2.1	--	V	VLCDX[2:0]=000
		--	2.3	--		VLCDX[2:0]=001
		--	2.5	--		VLCDX[2:0]=010
		--	2.7	--		VLCDX[2:0]=011
			2.9			VLCDX[2:0]=100
		--	3.1	--		VLCDX[2:0]=101
		--	3.3	--		VLCDX[2:0]=110
		--	3.5	--		VLCDX[2:0]=111
Ilcd	LCD charge pump current[2]	--	--	500	uA	
Digital I/O parameter						
IOL	Output low current sink	--	3	--	mA	VOL=0.3V, PTxSR=0
		--	12	--		VOL=0.3V, PTxSR=1
IOH	High output current source	--	3	--	mA	VOH=VDD-0.3V, PTxSR=0
		--	12	--		VOH=VDD-0.3V, PTxSR=1
VIH	Input high voltage	0.7VDD	--	--	V	
VIL	Input low voltage	--	--	0.3VDD	V	
VOH	Output high voltage	VDD-0.3	--	--	V	
VOL	Output low voltage	--	--	VSS+0.3	V	

Note:

1. Noise free bits and effective resolution are both related to the signal's full scale range. Its peak to peak or rms noise plays the decisive role.
2. The charge pump driving capability is related to the choice of capacitor and the operating frequency.

Packaging Information



Dimensions:mm

Symbol	Min.	Nom.	Max.
A	——	——	1.60
A1	0.05	——	0.20
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.19	——	0.27
c	0.13	——	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50BSC		
L	0.40	——	0.65
L1	1.00BSC		
θ	0	——	7

Fig 4. LQFP48 mechanical specification