SD8001

24 bits ADC SOC

Features

- High precision 24 bits ADC, 20 bits effective resolution, 3 differential or 6 single-ended inputs
- Low noise, high input impedance preamplifier with selectable gain: 1, 12.5, 50, 100, or 200; 40nVrms equivalent input noise, 16 bits noise free at ±4mV FSR
- 8 bits RISC ultra low power MCU, 200uA typical current, 1.5uA at standby, and less than 1uA at sleep
- Strong anti-interference capability, exceeds 4kV EFT test
- 16K Bytes OTP and 256 Bytes SRAM, support online OTP programming
- Multiple clock sources, flexible clock selection, external oscillator malfunction detection
- ADC output rate: 8SPS–2KSPS
- 12SEG X 4COM LCD drive, programmable boost module
- Built-in temperature sensor, supports single point calibration
- 1.2V low temperature drift voltage reference output
- Selectable voltage source: 2.4V/2.6V/2.9V/3.3V
- Flexible battery voltage detection range 2.0V-3.3V
- External or internal voltage reference for ADC, multiple internal voltage references
- RTC module calculates calendar/time information
- Abundant peripheral resources: UART, I2C, PDM, PFD, CAPTURE, TIMER
- Low voltage detection and power on reset circuit
- Operating voltage range: 2.4V to 3.6V
- Operating temperature range: -40℃ to 85℃

Description

The SD8001 is a CMOS SOC with built-in 24 bit ADC. It has very rich peripheral resources: RTC, UART, I2C, selectable voltage source to provide a stable excitation for external transducer, PGIA, voltage step-up module, timer with CAPTURE function, and PDM/PFD output. The internal 16K Bytes OTP program memory can be programmed online and can be used in place of external EEPROM.

Three working modes are provided so users can select the optimum choice between speed and power. They are normal mode, standby mode, and sleep mode.

The IC was designed with ultra low power technology. Operating at 2MHz clock and 3V supply, MCU itself consumes 200uA only. During typical operation, the total IC current is 600uA. Standby current at 32kHz clock is 1.5uA. At sleep mode, current is less than 1uA. Such low current consumption is very suitable for battery powered applications.

At 200X gain and 8SPS ADC output rate the equivalent input noise is 40nVrms. At ±4mV FSR the IC output is 16 bits noise free. With such noise performance the IC is ideal for electronic scale and similar applications where very weak signal from bridge sensor has to be processed.

The clock can come from external crystal oscillator or internal RC oscillator. Capacitors for the 32.768kHz crystal circuit are provided.

The LCD driver consumes ultra low power but has high driving capacity. Gray level adjustment is supported. The embedded programmable boost module allows brightness to be maintained during low voltage condition.

The RTC module calculates year, month, week, day, hour, minute, second, and automatically makes the leap year adjustment. Time precision can be adjusted by modifying the register through software.

The IC can determine if the external oscillator has stopped. If this happens the internal 2MHz RC oscillator is waken up and becomes the new clock source immediately. The IC functions continuously.

The IC has strong anti-interference capability. It passes 4kV Electrical Fast Transient (EFT) test easily without using any additional protective circuit, and is suitable for harsh environment applications.

Applications

Pricing scale, jewelry scale, other high precision scales

Ordering Information

Bare die or custom made PCB module

Pin Diagram and Descriptions

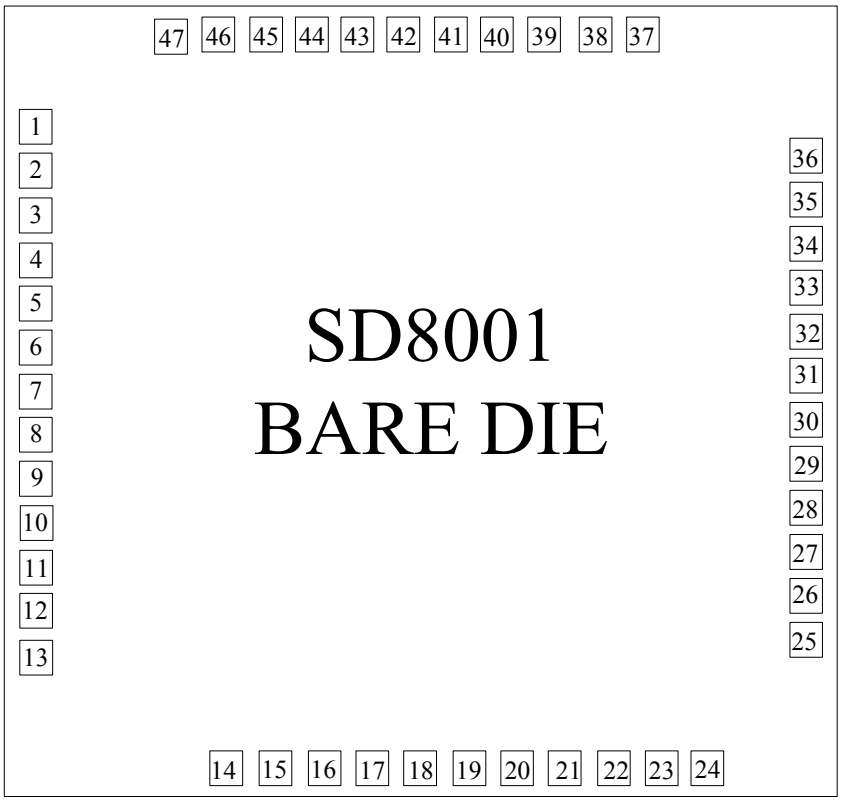

Figure 1. Pad diagram

Table 1. Pad Descriptions

Pad No.	PAD Name	Attribute	Description
2,1	CP，CN	Analog	External capacitor connection pins for the voltage booster circuit. Capacitor not needed if high frequency RC clock is used for the booster.
3	VLCD	Analog	LCD driver power supply, internally connect to DVDD or booster output through register secting, connect 1uF filter capacitor to DVDD
4	ACM	Analog	1.2V reference output, floating when ACM is shutdown, connect 0.1uF cap to AVSS
5-10	AI0--AI5	Analog input	Analog signal inputs, each port has an independent register controlled pull-down resistor(default OFF), should be ON for unused port; AI0-AI1, AI2-AI3, AI4-AI5 can be set as 3 differential or 6 single-ended inputs; AI0-AI1 can also be set as ADC's external reference input pair; AI2-AI3 can also be set to bypass the preamp and connect to ADC inputs directly

11	AVDDR	Analog	Internal LDO output for IC's analog module, can provide excitation to external transducer, connect 0.1uF-10uF filter capacitor to AVSS
12	AVDD	Power	Analog supply voltage, connect 0.1uF capacitor to AVSS
13	AVSS	Ground	Analog ground
14-15	XIN/P50-- XOUT/P51	Analog , I/O	XIN, XOUT: crystal oscillator pins, connect to 32.768kHz or 1MHz-6MHz crystals through register set up, XIN can be the external clock input when not using crystal; Digital I/O port P50-P51
16-17	LBTIN/RX/P52-- LBTVSS/TX/P53	Analog , I/O	LBTIN, LBTVSS: low battery detect, LBTVSS should be floating when using ADC to perform this measurement; UART data receive RX and transmit TX; Digital port P52-P53
18	CCP1/P54	I/O	CAPTURE1 CCP1 input or digital port P54
19	PDM0/P55	I/O	Pulse density modulation PDM0 output or digital port P55
20	BUZ/P27	I/O	Buzzer BUZ output or digital port P27
21	DVDDR	Analog	Internal LDO output for digital circuits, can connect to DVDD when not used
22	DVDD	Power	Digital supply voltage, connect 0.1uF capacitor to DVSS
23	DVSS	Ground	Digital ground
24	RST_B/VPP	I	Reset pin, active low, also used as OTP high voltage programming pin
25	CCP0/P26	I/O	CAPTURE0 CCP0 input or digital port P26
26	T0CK/P25	I/O	TIMER0 external clock T0CK input or digital port P25
27	PFD/P24	I/O	Programmable frequency divider PFD output or digital port P24
28-29	SCL/P23-- SDA/P22	I/O	I^2C clock SCL and data SDA or digital port P23-P22
30	INT1/P21	I/O	External interrupt1 INT1 or digital port P21
31	INT0/P20	I/O	External interrupt0 INT0 or digital port P20
32-43	SEG11/P47-- SEG0/P34	I/O	LCD SEG11-SEG0 or digital port P47-P40, P37-P34
44-47	COM3/P33-- COM0/P30	I/O	LCD COM3-COM0 or digital port P33-P30

Remark: All I/O ports Pnn have internal pull-up option (default OFF) and input hysteresis at 0.3VDD/0.7VDD.

Functional Block

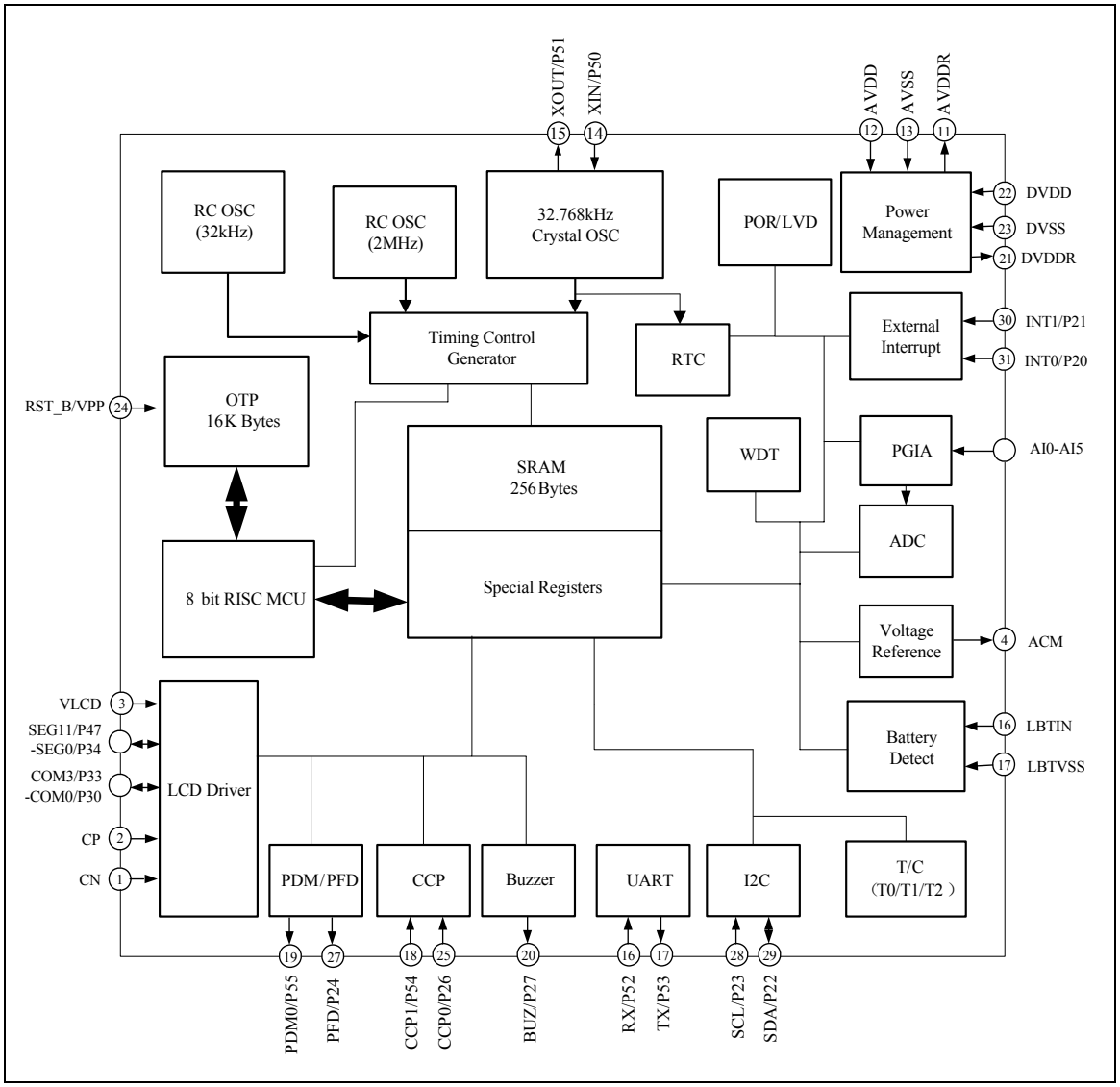

Figure 2. Functional block diagram

Typical Applications

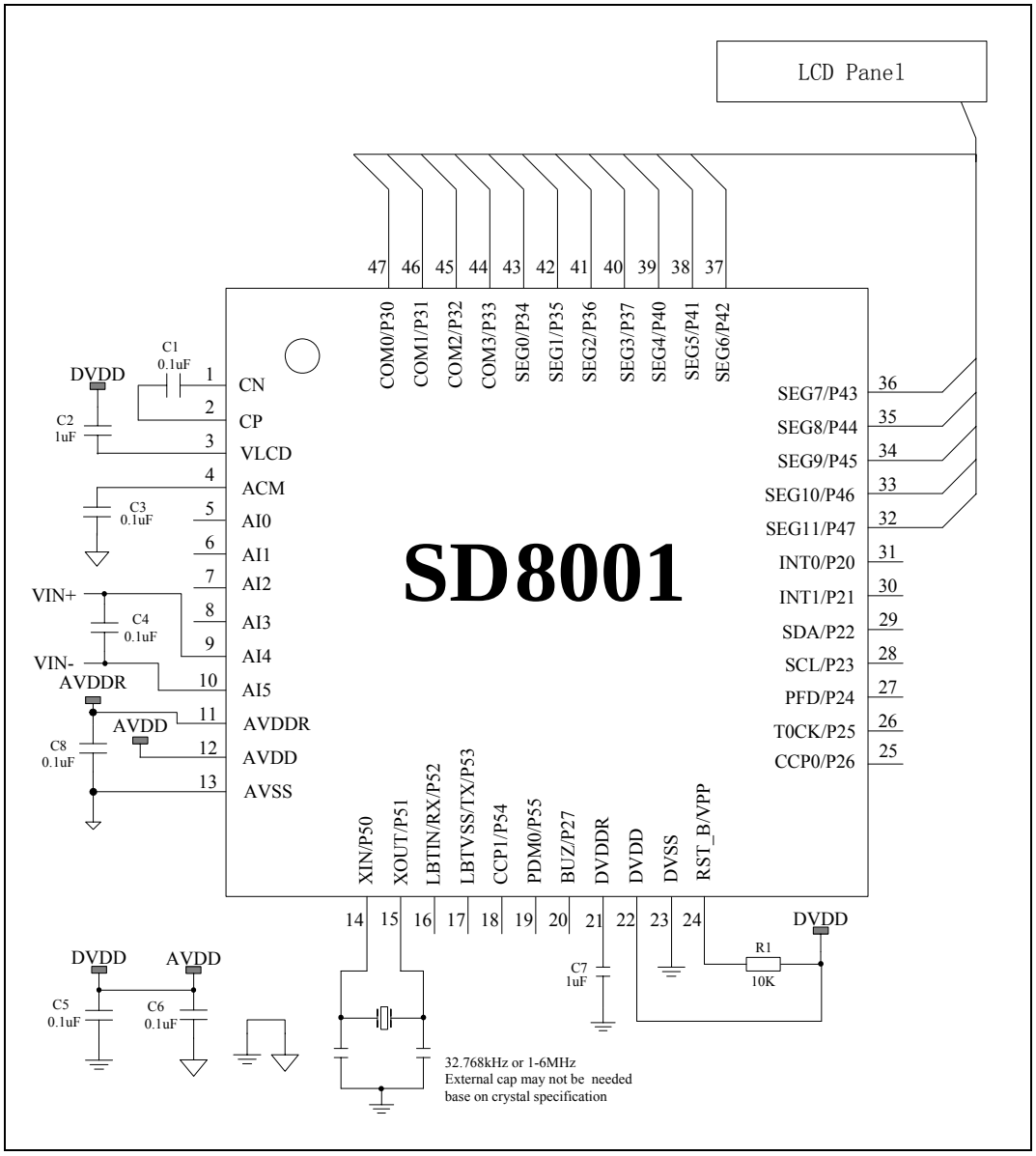

Figure 3. Typical application diagram

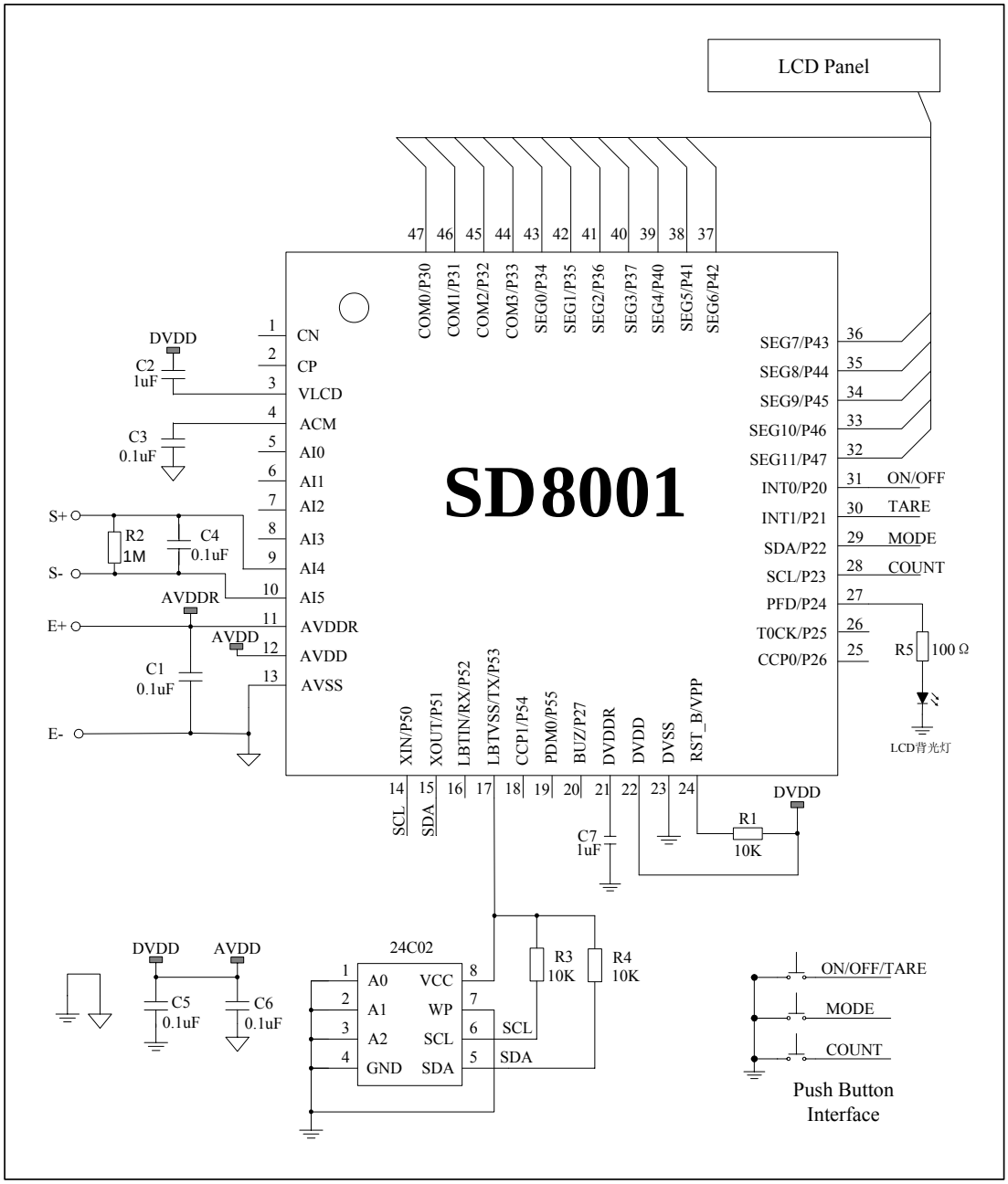

Figure 4. Kitchen scale typical application diagram

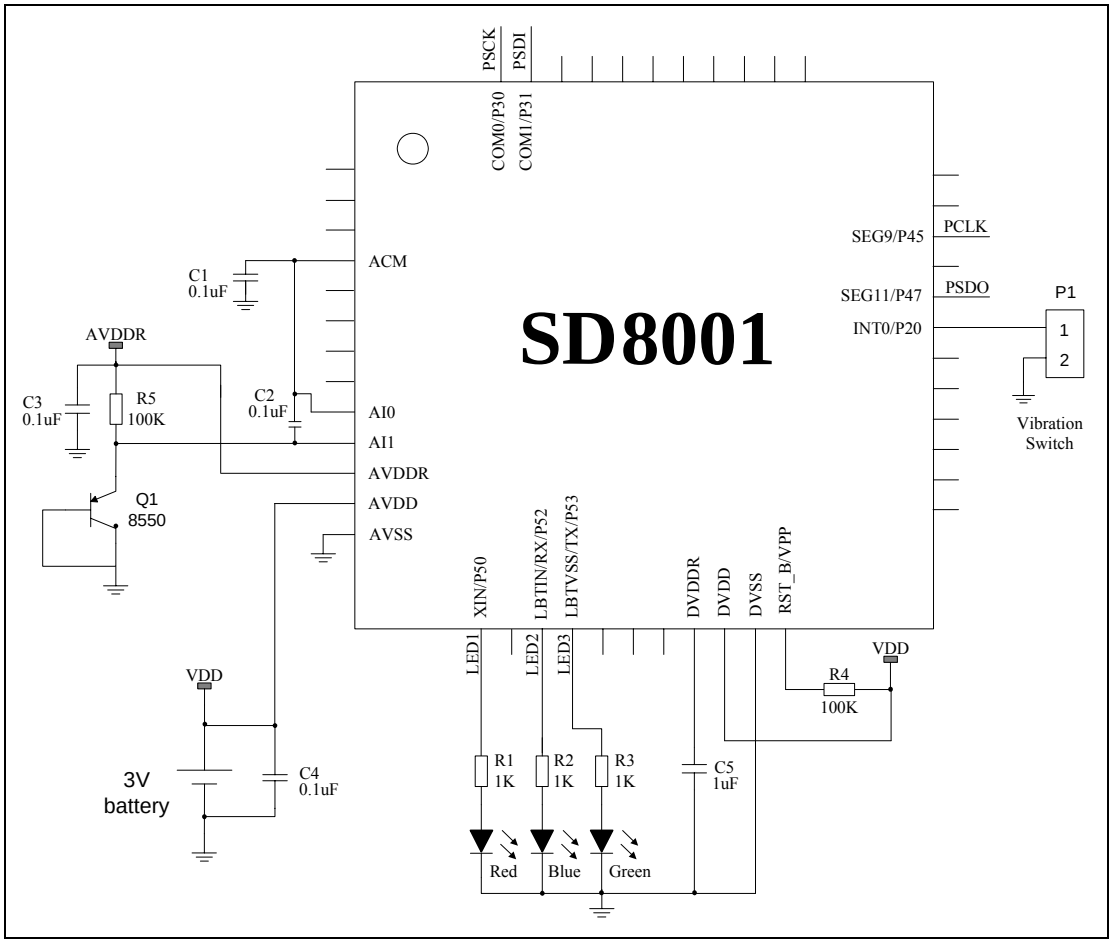

Figure 5. Temperature measurement typical application diagram

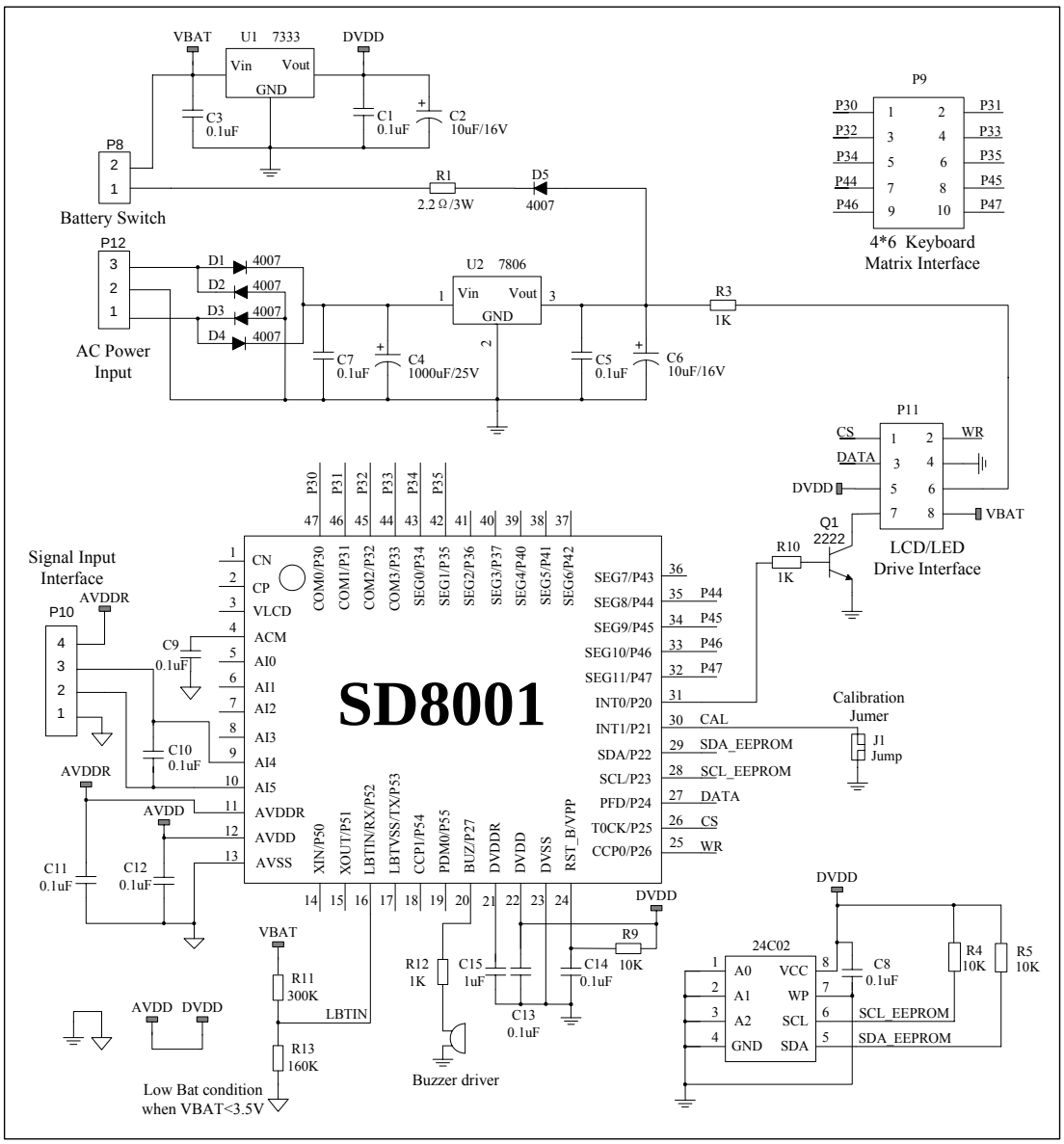

Figure 6. Pricing scale typical application diagram

Electrical Specifications

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
T_A	Operating temperature	-40	+85	°C
T_S	Storage temperature	-55	+150	°C
V_{DD}	Supply voltage	-0.2	+4.0	V
Vpp	Programming voltage	-0.2	+7.5	V
V_{IN}, V_{OUT}	Digital input/output voltage	-0.2	V_{DD}+0.3	V
T_L	Reflow temperature profile	Per IPC/JEDECJ-STD-020C		°C

Remarks:
1. CMOS device can easily be damaged by electrostatics. It must be stored in conductive foam, and careful not to exceed the operating voltage range.
2. Turn off power before insert or remove the device.

Table 3. Electrical Specifications（VDD=3V, T_A=25℃）

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Remarks
VDD	Supply voltage	2.4	3.0	3.6	V	Analog modules operating voltage
		2.0	3.0	3.6		Digital modules and MCU operating voltage
FOSC	Operating frequency	16k	2M	--	Hz	
IHRC	Internal high frequency RC oscillator	1.9	--	2.1	MHz	
ILRC	Internal low frequency RC oscillator	28	--	36	kHz	
HXT	External high frequency crystal oscillator	1	--	6	MHz	
LXT	External low frequency crystal oscillator	16	--	--	kHz	
IDD1	Operating current 1	--	630	--	uA	2MHz crystal for MCU Digital modules supply from DVDDR Analog modules active
IDD2	Operating current 2	--	350	--	uA	2MHz internal RC oscillator for MCU Digital modules supply from DVDD Analog modules inactive
		--	320	--		2MHz crystal for MCU Digital modules supply from DVDD Analog modules inactive
IDD3	Operating current 3	--	210	--	uA	2MHz internal RC oscillator for MCU Digital modules supply from DVDDR Analog modules inactive
		--	200	--		2MHz crystal for MCU Digital modules supply from DVDDR Analog modules inactive

IDD4	Operating current 4	--	9	--	uA	32.768kHz crystal for MCU Digital modules supply from DVDD Analog modules inactive
		--	7	--		32.768kHz internal RC oscillator for MCU Digital modules supply from DVDD Analog modules inactive
IDD5	Operating current 5	--	3	--	uA	32.768kHz crystal for MCU MCU at standby mode Analog modules inactive
		--	1.5	--		32.768kHz internal RC oscillator for MCU MCU at standby mode Analog modules inactive
IDD6	Operating current 6	--	0.2	1	uA	MCU at sleep mode Analog modules inactive
Fsam	ADC sampling rate	128	--	256	kHz	
OSR	Over sampling rate	128	--	16384		
NFbit	Noise free bits[1]	--	16	TBD	bits	Gain=200，input FSR=±4mV
NMbit	No missing code output	--	--	24	bits	
INL	INL	--	0.002	--	%FSR	
VINdif	PGIA differential input range	--	--	1800	mV	1X gain
		-Vref/12.5	--	Vref/12.5		12.5X gain
		-Vref/50	--	Vref/50		50X gain
		-Vref/100	--	Vref/100		100 X gain
		-Vref/200	--	Vref/200		200 X gain
VIN	PGIA input voltage range[2]	-0.3	--	AVDDR		1X gain and buffer is off
		0.3	--	AVDDR-0.7		1X gain and buffer is on, or gain≠1
Nrms	RMS noise	--	40	--	nVrms	200X gain
Vacm	ACM voltage output	--	1.2	--	V	
IacmSour	ACM current source	--	1	--	mA	
IacmSink	ACM current sink	--	1	--	mA	
PSRacm	ACM PSR	--	100	--	uV/V	
Tgain	Gain tempco	--	±4	--	ppm/℃	-10℃ to +40℃
Vavddr	AVDDR Voltage output	--	2.4	--	V	avddrx[1:0]=00
		--	2.6	--		avddrx[1:0]=01
		--	2.9	--		avddrx[1:0]=10
		--	3.3	--		avddrx[1:0]=11
Iavddr	AVDDR current	--	10	--	mA	Output current strength
POR	POR voltage	--	2.0	--	V	Power on reset threshold

LVD	LVD voltage	--	1.9	--	V	Low voltage reset threshold
THlbt	LVD hysteresis	--	200	--	mV	Low voltage reset threshold
Vlbt	Low VDD alarm threshold	--	3.3	--	V	lbtx[3:0]=0010
		--	3.2	--		lbtx[3:0]=0011
		--	3.1	--		lbtx[3:0]=0100
		--	3.0	--		lbtx[3:0]=0101
		--	2.9	--		lbtx[3:0]=0110
		--	2.8	--		lbtx[3:0]=0111
		--	2.7	--		lbtx[3:0]=1000
		--	2.6	--		lbtx[3:0]=1001
		--	2.5	--		lbtx[3:0]=1010
Vlbt	Low VDD alarm threshold	--	2.4	--	V	lbtx[3:0]=1011
		--	2.3	--		lbtx[3:0]=1100
		--	2.2	--		lbtx[3:0]=1101
		--	2.1	--		lbtx[3:0]=1110
		--	2.0	--		lbtx[3:0]=1111
Vlcd	LCD charge pump output voltage	--	2.1	--	V	vlcdx[2:0]=000
		--	2.3	--		vlcdx[2:0]=001
		--	2.5	--		vlcdx[2:0]=010
		--	2.7	--		vlcdx[2:0]=011
		--	2.9	--		vlcdx[2:0]=100
		--	3.1	--		vlcdx[2:0]=101
		--	3.3	--		vlcdx[2:0]=110
		--	3.5	--		vlcdx[2:0]=111
Ilcd	LCD charge pump current[3]	--	--	500	uA	Output current strength
Digital I/O parameter						
IOL	Output low current sink	--	2	--	mA	VOL=0.3V, PTxSR=0
		--	10	--		VOL=0.3V, PTxSR=1
IOH	High output current source	--	2	--	mA	VOH=VDD-0.3V, PTxSR=0
		--	10	--		VOH=VDD-0.3V, PTxSR=1
VIH	Input high voltage	0.7VDD	--	--	V	
VIL	Input low voltage	--	--	0.3VDD	V	
VOH	Output high voltage	VDD-0.3	--	--	V	
VOL	Output low voltage	--	--	VSS+0.3	V	

Note:

1. Noise freebits and effective resolution are both related to the signal's full scale range. Its peak to peak or rms noise plays the decisive role.
2. The signal input range is limited by the differential signal input range and the absolute voltage at the input terminals. The first one is the real signal input range. It is affected by the PGIA gain and the ADC voltage reference choice. The second one includes both differential and common mode components and is mainly limited by the circuit.
3. The charge pump driving capability is related to the choice of capacitor and the operating frequency.