SD3101F

3 Diff Channels Meterage and Signal Detection ASIC

Features

- High precision 24 bits ADC, selectable gain, 3 differential or 5 pseudo-differential inputs
- Measures true RMS value, extrema, and frequency
- Built-in calibration and arithmetic functions to calculate the measured values automatically
- 256 bytes internal OTP for constant type data storage
- UART and I^2C ports, support 4 bits device address
- PFD or PWM output
- 1.16V low TC voltage reference output
- Can select external low frequency crystal or internal RC oscillator
- RTC module together with external 32.768kHz crystal provides calendar/time information including leap year, timing accuracy is adjustable
- Operating voltage range: 2.5V~ 3.6V
- Operating temperature range: -40℃~ 85℃

Description

SD3101F is a meterage and signal detection ASIC with built-in 24 bits ADC. Input channels can be set as three differentials or five pseudo-differentials. Input gain is selectable at 1, 2, 8, or 16.

AC true RMS or DC signals are measured directly. AC signal does not have to go through external rectification circuit.

ADC data output rate is selectable for appropriate choice between speed and precision.

The chip is highly integrated. Very few external components are needed for AC/DC voltmeter or current meter realization.

Three working modes are available: normal, standby, and sleep modes. Their typical current consumptions are 1.2mA, 7.6uA, and ≤3uA.

The IC passes 4kV Electrical Fast Transient (EFT) test easily without using any additional protection circuit. It is suitable for applications in harsh environment.

Applications

- Single or three phases AC voltmeter or current meter
- Single or three pairs DC voltmeter or current meter
- Multi-channel low frequency signal detection instrumentation

Ordering Information

SSOP24 package

Pin Diagram and Descriptions

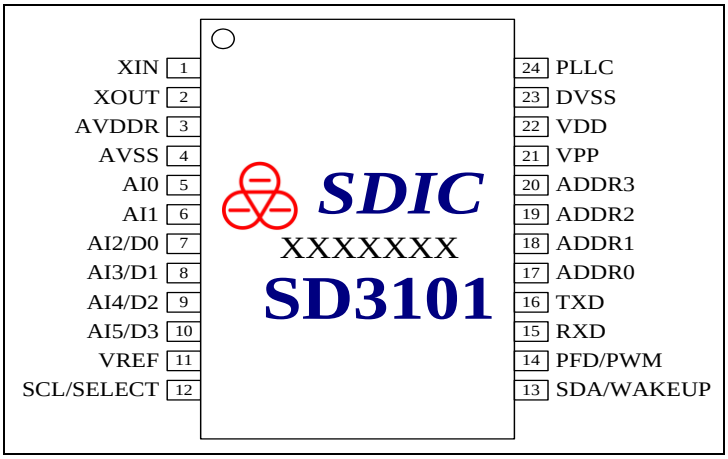


Figure 1. Pin out diagram

Table 1. Pin Descriptions

Pin No.	Pin Name	Attribute	Descriptions
1	XIN	Analog	Crystal oscillator input
2	XOUT	Analog	Crystal oscillator input
3	AVDDR	Analog	Internal LDO output for IC's analog module, connect 1uF capacitor to AVSS
4	AVSS	Ground	Analog ground
5-6	AI0-AI1	Analog input	Analog signal differential or two pseudo-differential inputs
7-10	AI2/D0-AI5/D3	Analog input Digital output	Two analog differential or four pseudo-differential inputs, or digital output port D0-3. Default are all analog inputs
11	VREF	Analog	1.16V reference voltage for ADC, can connect to external reference source, connect 100pF and 10uF capacitor to AVSS
12	SCL/SELECT	Digital input	I^2C port SCL or communication SELECT command input
13	SDA/WAKEUP	I/O	I^2C port SDA or WAKEUP command input
14	PFD/PWM	Digital output	PFD/PWM output
15	RXD	Digital input	UART port RXD
16	TXD	Digital output	UART port TXD
17-20	ADDR0-3	Digital input	Device address with internal pull-up and input hysteresis at 0.3VDD/0.7VDD.
21	VPP	Analog	OTP high voltage programming pin, connect 1uF capacitor to DVSS
22	VDD	Power	Power supply for the IC, connect 0.1uF to DVSS
23	DVSS	Ground	Digital ground
24	PLLC	Analog	PLL capacitor, connect 1nF to DVSS

Functional Block

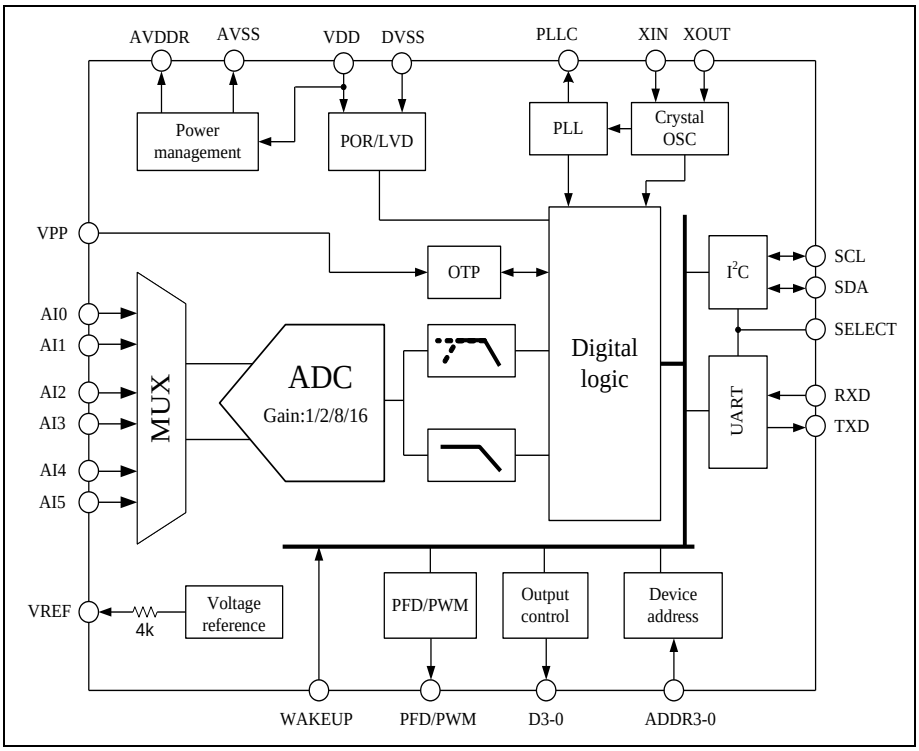


Figure 2. Functional block diagram

System Setting

Table 2. SYSTEM Register

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYSTEM(0x00)	pken	sleep	AVDDR [1:0]		hour_sel	--		
R/W	R/W	R/W	R/W		R/W	--		
Reset	0	0	10		0	--		

pken – Extrema measurement enable

1 – enable extrema measurement

0 – disable extrema measurement, extrema are reset (default)

sleep – sleep mode control

1 – set IC to sleep mode

0 – set IC to normal operation (default)

AVDDR[1:0] – AVDDR output voltage select

00 – 2.4V

01 – 2.7V

10 – 3.0V (default)

11 – 3.3V

hour_sel – RTC 12/24 hour format select

1 – 24 hours format

0 – 12 hours format (default)

Table 3. PORTCON Register

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PORTCON(0x01)	--				AIEN[3:0]			
R/W	--				R/W			
Reset	--				1111			

AIEN[3:0] – AI5/D3-AI2/D0 ports function select

1 – set to analog input ports (default)

0 – set to digital output ports

ADC Setting

Table 4. ADCMUX Register

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCMUX(0x02)	--	ADINPS[2:0]			--	ADINNS[2:0]		
R/W	--	R/W	R/W	R/W	--	R/W	R/W	R/W
Reset	--	0	0	0	--	0	0	0

ADINPS[2:0]：ADC positive input terminal select

000：A0
001：A1
010：A2
011：A3
100：A4
101：A5
110：reserved
111：reserved

ADINNS[2:0]：ADC negative input terminal select

000：A0
001：A1
010：A2
011：A3
100：A4
101：A5
110：reserved
111：reserved

Table 5. ADCCON Register

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCCON(0x03)	hpf_en	OSR[2:0]			GAIN[1:0]		ac_dc	adc_en
R/W	R/W	R/W			R/W		R/W	R/W
Reset	1	011			00		0	0

hpf_en – high pass filter enable

1 – enable high pass filter (default)
0 – disable high pass filter

OSR[2:0] – DC measurement oversample rate select (AC measurement uses fixed rate).

000 – 128
001 – 256
010 – 512
011 – 1024 (default)
100 – 2048
101 – 4096
110 – 8192
111 – 16384

GAIN[1:0] – ADC gain select

00 – 1 (default)
01 – 2
10 – 8
11 – 16

ac_dc – measurement mode

1 – AC measurement
0 – DC measurement (default)

adc_en – ADC enable

1 – enable ADC
0 – disable ADC (default)

Table 6. Data Output Port Registers[1]

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADC_DATAU（0x04）	ADC data, upper byte							
ADC_DATAH（0x05）	ADC data, middle byte							
ADC_DATAL（0x06）	ADC data, lower byte							
SCALED _DATAU（0x07）	Measured value, upper byte [2]							
SCALED _DATAH（0x08）	Measured value, middle byte							
SCALED _DATAL（0x09）	Measured value, lower byte							
PKMAXH（0x0A）	High extremum, upper byte							
PKMAXL（0x0B）	High extremum, lower byte							
PKMINH（0x0C）	Low extremum, upper byte							
PKMINL（0x0D）	Low extremum, lower byte							
FREQ_H（0x0E）	frequency value, upper byte							
FREQ_L（0x0F）	frequency value, lower byte							

Remarks:
1. All registers in this table are for read only.
2. Refer to equation 1 in the Calibration section.

Digital Output Port Setting

Table 7. Digital Output Port Register

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DOUT(0x10)					D3	D2	D1	D0
R/W					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Dx – digital output port output voltage level

1 – output high voltage level

0 – output low voltage level (default)

PWM Setting

Table 8. PWMCON Register

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMCON (0x11)	pwm_en	--					pwmclk_sel [1:0]	
R/W	R/W	--					R/W	
Reset	0	--					00	

pwm_en – PWM enable

1 – enable PWM

0 – disable PWM (default)

pwmclk_sel [1:0] – PWM clock select

00 – MCLK (system operating frequency 2.097MHz) (default)

01 – MCLK / 4

1x – MCLK / 16

Table 9. PWM Registers

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM_DH（0x12）	PWM clock cycles for PWM pulse high voltage level, upper byte							
PWM_DL（0x13）	PWM clock cycles for PWM pulse high voltage level, lower byte							
PWM_CH（0x14）	PWM clock cycles for PWM frequency, upper byte							
PWM_CL（0x15）	PWM clock cycles for PWM frequency, lower byte							

PWM pulse high voltage level duration is (PWM_DH:DL + 1)/PWMCLK_SEL.

PWM frequency is PWMCLK_SEL / (PWM_CH:CL + 1).

PWM_DH:DL just be less than or equal to PWM_CH:CL.

Real Time Clock

When connected with external low frequency crystal oscillator (32.768kHz), the IC can provide accurate data on year, month, week, date, hour, minute, and second.

Table 10. RTC Registers

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SECOND (0x16)	--	S40	S20	S10	S8	S4	S2	S1
MINUTE(0x17)	--	M40	M20	M10	M8	M4	M2	M1
HOUR(0x18)	--	--	H20	H10	H8	H4	H2	H1
DAY(0x19)	--	--	D20	D10	D8	D4	D2	D1
WEEK(0x1A)	--	--	--	--	--	W4	W2	W1
MONTH(0x1B)	--	--	--	M10	M8	M4	M2	M1
YEAR(0x1C)	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1

SECOND, MINUTE

Second and minute registers in BCD format from 00 to 59. For example, when the register read 0101 1001, the value is 59 in decimal unit.

HOUR

In the 24 hours format, Bit5 shows the H20 value. In the 12 hours format, Bit5 indicates current time is AM (Bit5=0) or PM (Bit5=1).

Table11 shows the HOUR values corresponding to the 24 or 12 hours display formats.

Table 11. HOUR[5:0] Values

24 Hours Format	12 Hours Format	24 Hours Format	12 Hours Format
00	12（AM12）	12	32（PM12）
01	01（AM01）	13	21（PM01）
02	02（AM02）	14	22（PM02）
03	03（AM03）	15	23（PM03）
04	04（AM04）	16	24（PM04）
05	05（AM05）	17	25（PM05）
06	06（AM06）	18	26（PM06）
07	07（AM07）	19	27（PM07）
08	08（AM08）	20	28（PM08）
09	09（AM09）	21	29（PM09）
10	10（AM10）	22	30（PM10）
11	11（AM11）	23	31（PM11）

DAY, MONTH, YEAR

The above three registers are all in BCD format. YEAR shows the year's last two digits only from 00 to 99.

WEEK

Table12 shows the WEEK values

Table 12. WEEK[2:0] Values

W4W2W1	Week	Remark	W4W2W1	Week	Remark
000	Sunday	0x00	100	Thursday	0x04
001	Monday	0x01	101	Friday	0x05
010	Tuesday	0x02	110	Saturday	0x06
011	Wednesday	0x03	111	--	--

Communication Port

SD3101F provides UART and I^2C communication options. Choose the option by setting the SELECT pin as shown in table 13 before applying power to the IC.

Table 13. Communication Port Select

SELECT pin	Communication Port
0	UART
1	I^2C

UART communication port data:

- Baud rate: 9600
- Data: 8bits
- Stop: 1bit
- Parity: None

Maximum baud rate for I^2C is 100kHz. After sending out an I^2C command, one has to wait 100ms before reading the response command. The E^2PROM address for sending command and response command are both starting at 0x00.

Note that the SELECT pin is read once only at the beginning of power on. The communication option is then set and cannot be changed until the IC is power off and on again.

Command Format

A complete command frame is shown in table 14. All values are in hex unit. Serial port format: 8 data bits, 1 stop bit, check digit (optional).

Table 14. Command Frame Format

Command:	XX	XX	XX XX……XX	CRC16
Remarks:	Device address	Control code	Command parameters	Check bytes

The CRC16 generator polynomial is $X^{16} + X^{15} + X^2 + 1$. The upper byte is sent first. The upper bit of each byte is sent first.

When the master device is sending a frame over, the time between two adjacent bytes should not exceed 3 times the byte transmission time (3ms), otherwise the frame transmission would be considered as completed.

Device Address Description

The device address is 8 bits long as shown in table 15. Bit 3:1 are fixed at 0. A maximum of 14 different addresses is allowed.

Table 15. Device Address Setup

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
addr3	addr2	addr1	addr0	0	0	0	r/w

r/w — I^2C read/write control bit (internally set to 0 if UART is selected)

1 – read

0 – write

0x00 is a common address (UART only). All devices can use this address for communication. This setup is suitable for single slave device system.

0xFF is a broadcast address (UART only). When using the broadcast address, the slave device does not have to response.

Command Operation Description

1. Write Register

Master write to register command is shown in figure 3. The slave response is shown in figure 4.

Device Address (8 bits)	Control Code (8 bits)	Register Address (8 bits)	Number of Bytes N (8 bits)	Register Data (N * 8 bits)	CRC Check (16 bits)

Figure 3. Master writes to slave register

Example:

Send Command	00 01 00 01 00 24 6C
Remarks	00 device address
	01 Write Register command
	00 register address
	01 number of bytes
	00 data written to register
	24 6C CRC check

Device Address (8 bits)	Control Code (8 bits)	Response Code (8 bits)	CRC Check (16 bits)

Figure 4. Slave responses

Example:

Response Command	00 01 00 70 50
Remarks	00 device address
	01 Write Register command
	00 response code
	70 50 CRC check

Response code:

0x00 - success

0x01 - address exceeds boundary

0x02 - number of data bytes exceed boundary

0x03 - data error

If there is error in the response command, the command code will be OR'ed with 0x80 to indicate error.

2. Read Register

Master read from slave register command is shown in figure 5. The slave response is shown in figure 6.

Device Address (8 bits)	Control Code (8 bits)	Register Address (8 bits)	Number of Bytes N (8 bits)	CRC Check (16 bits)

Figure 5. Master read from slave register

Example:

Send Command	00 02 00 01 60 24
Remarks	00 device address
	02 Read Register command
	00 register address
	01 number of bytes
	60 24 CRC check

Device Address (8 bits)	Control Code (8 bits)	Number of Bytes N (8 bits)	Register Data (N * 8 bits)	CRC Check (16 bits)

Figure 6. Slave responses

Example:

Response Command	00 02 01 00 A0 74
Remarks	00 device address
	02 Read Register command
	01 number of bytes
	00 data in register or OTP
	A0 74 CRC check

If there is error in the response command, the command code will be OR'ed with 0x80 to indicate error.

3. Write OTP

Master write to OTP command is shown in figure 7. The slave response is shown in figure 8.

Device Address (8 bits)	Control Code (8 bits)	OTP Address (8 bits)	Number of Bytes N (8 bits)	OTP Data (N * 8 bits)	CRC Check (16 bits)

Figure 7. Master writes to slave OTP

Example:

Send Command	00 03 00 01 00 25 D4
Remarks	00 device address
	03 Write OTP command
	00 register address
	01 number of bytes
	00 data written to OTP
	25 D4 CRC check

N must be 15 or less.

Device Address (8 bits)	Control Code (8 bits)	Response Code (8 bits)	CRC Check (16 bits)

Figure 8. Slave responses

Example:

Response Command	00 03 00 71 30
Remarks	00 device address
	03 Write OTP command
	00 response code
	71 30 CRC check

Response code:

0x00 - success

0x01 - address exceeds boundary

0x02 - number of data bytes exceed boundary

0x03 - data error

0x04 – write OTP error

If there is error in the response command, the command code will be OR'ed with 0x80 to indicate error.

4. Read OTP

Master read from slave OTP command is shown in figure 9. The slave response is shown in figure 10.

Device Address (8 bits)	Control Code (8 bits)	OTP Address (8 bits)	Number of Bytes N (8 bits)	CRC Check (16 bits)

Figure 9. Master read from slave OTP

Example:

Send Command	00 04 00 01 80 25
Remarks	00 device address
	04 Read OTP command
	00 register address
	01 number of bytes
	80 25 CRC check

N must be 15 or less.

Device Address (8 bits)	Control Code (8 bits)	Number of Bytes N (8 bits)	OTP Data (N * 8 bits)	CRC Check (16 bits)

Figure 10. Slave responses

Example:

Response Command	00 04 01 00 40 75
Remarks	00 device address
	04 Read OTP command
	01 number of bytes
	00 data in OTP
	40 75 CRC check

If there is error in the response command, the command code will be OR'ed with 0x80 to indicate error.

5. Calibration

Master calibrates slave command is shown in figure 11. The slave response is shown in figure 12.

Device Address (8 bits)	Control Code (8 bits)	Number of Bytes = 2 (8 bits)	Ideal Measured Value (2 * 8 bits)	CRC Check (16 bits)

Figure 11. Master calibrates slave

Example:

Send Command	00 05 02 01 25 45 47
Remarks	00 device address
	05 Calibration command
	01 25 Ideal measured value
	45 47 CRC check

Device Address (8 bits)	Control Code (8 bits)	Response Code (8 bits)	CRC Check (16 bits)

Figure 12. Slave responses

Example:

Response Command	00 05 00 72 90
Remarks	00 device address
	05 Calibration command
	00 response code
	72 90 CRC check

Response code:

0x00 - success

0x03 - data error

Calibration

The master device can request SD3101F to perform calibration function by sending the 0x05 control code to the IC. After calibration, the master can read the measured value (SCALED_DATAU/H/L) directly without having to perform calculation on the ADC raw data.

One should first apply the calibration signal to the selected analog input pair. As shown in figure 11, during calibration, one should send to the IC the ideal measured value. Based on the ideal measured value，ADC setting, and the measured calibration signal value, the IC will generate and save the calibration factor. SD3101F can repeat the calibration based on different ADC settings and different calibration signals for up to 128 times.

The calibration factor is two bytes long. The measured value calculation is shown in equation (1).

$$\text{Measured value} = \text{ADC data} * \text{calibration factor} \qquad (1)$$

ADC setting includes ADCMUX (table 4) and ADCCON (table 5). The IC performs calibration base on this setting. When the master device reads the measured value during normal operation, the present ADCMUX and ADCCON setting must be the same as the one used during calibration.

The ideal measured value entered at calibration is the complete number without the decimal point. For example, when the calibration signal is 1.000V, the ideal measured value entered should be 1000 instead of 1; when the calibration signal is 10.00V, the ideal measured value entered should be 1000 instead of 10; when the calibration

signal is 999.9V, the ideal measured value entered should be 9999 instead of 999; when the calibration signal is 1000V, the ideal measured value entered should be 1000.

OTP

256 bytes of internal OTP are reserved for user. One can use them to save ID or other constants.

The master device issues command codes 0x03 and 0x04 to write and read these OTP. The address range is 0x00 to 0xFF。

Please note that each OTP address can only be written once. They cannot be re-write.

Sleep and Wakeup

Setting SYSTEM register's bit 6 to one sends the IC into sleep mode. Note that sleep mode is available for UART communication setting only.

Pulling the WAKEUP pin low for 100us or longer will wake up the sleeping IC as shown in figure 13.

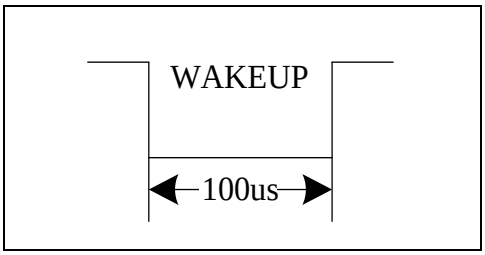


Figure 13. Wakeup timing diagram

Typical Application

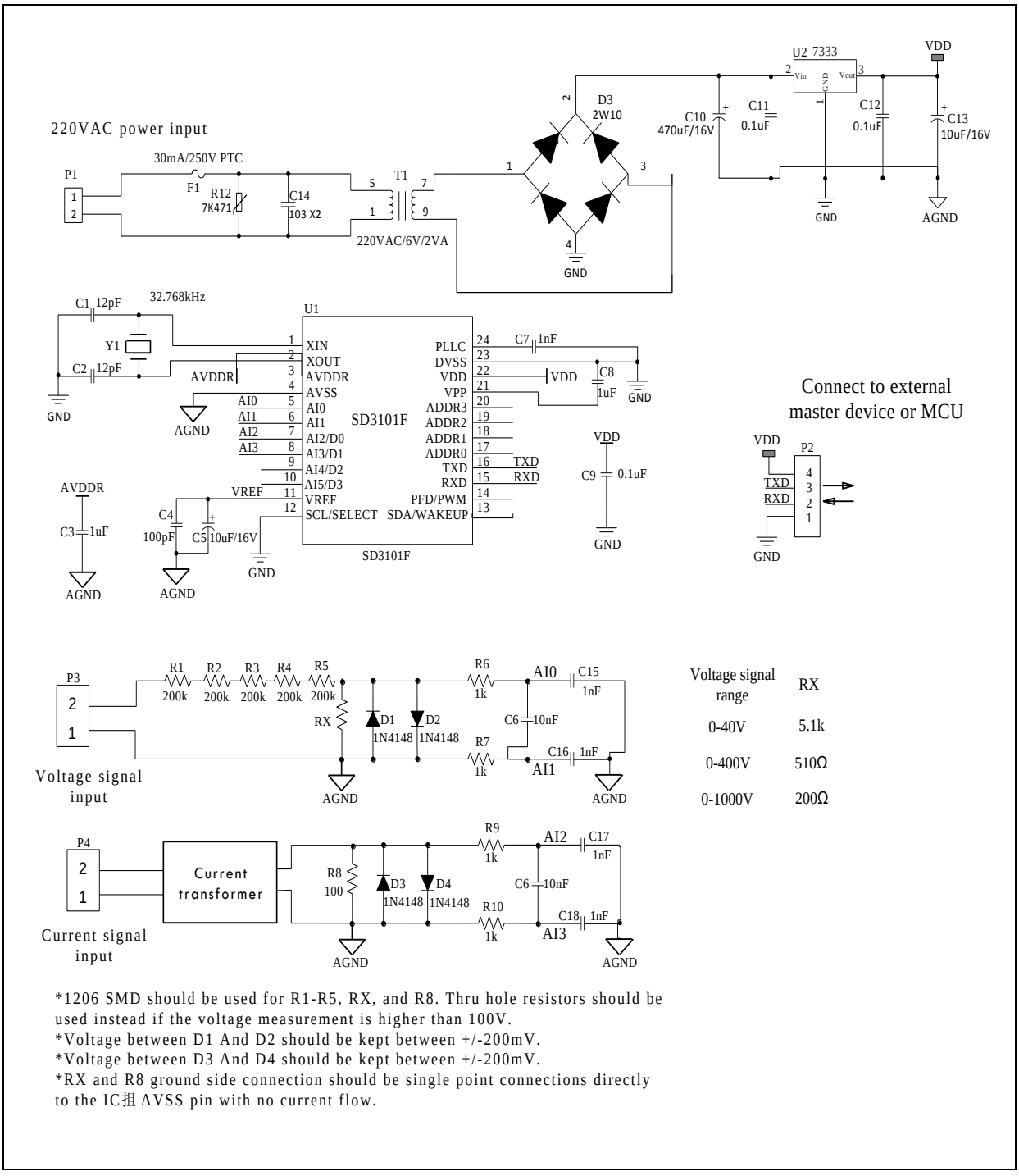
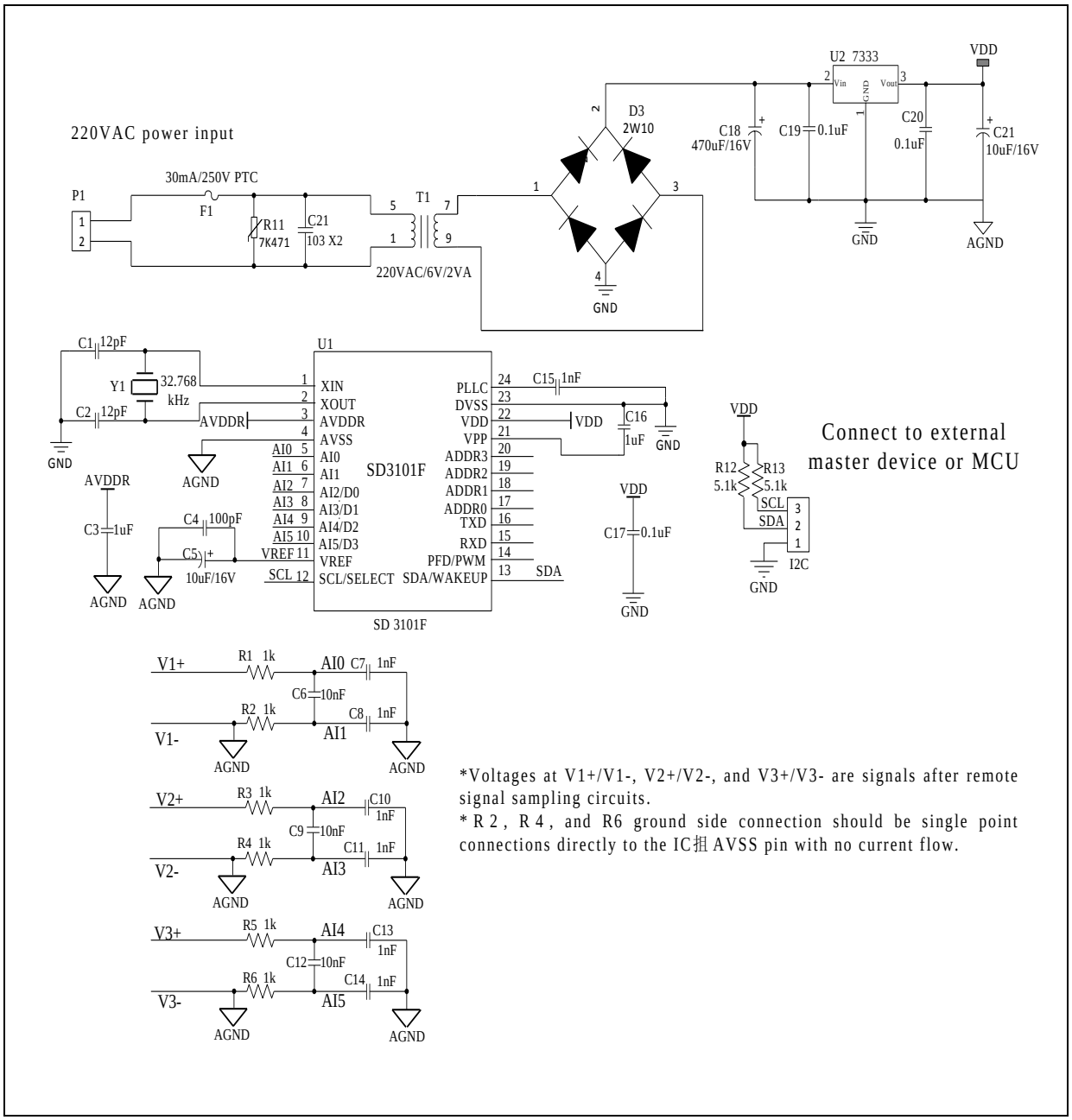


Figure 14. Single phase voltage meter/current meter with UART typical application diagram



*Voltages at V1+/V1-, V2+/V2-, and V3+/V3- are signals after remote signal sampling circuits.

*R2, R4, and R6 ground side connection should be single point connections directly to the IC担AVSS pin with no current flow.

Figure 15. Three phases voltage meter/current meter with I2C typical application diagram

Electrical Specifications

Table 16. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
T_A	Operating temperature	-40	+85	℃
T_S	Storage temperature	-55	+150	℃
V_{DD}	Supply voltage	-0.2	+4.0	V
Vpp	Programming voltage	-0.2	+7.5	V
V_{IN}, V_{OUT}	Digital input/output voltage	-0.2	V_{DD}+0.3	V
T_L	Reflow temperature profile	Per IPC/JEDECJ-STD-020C		℃

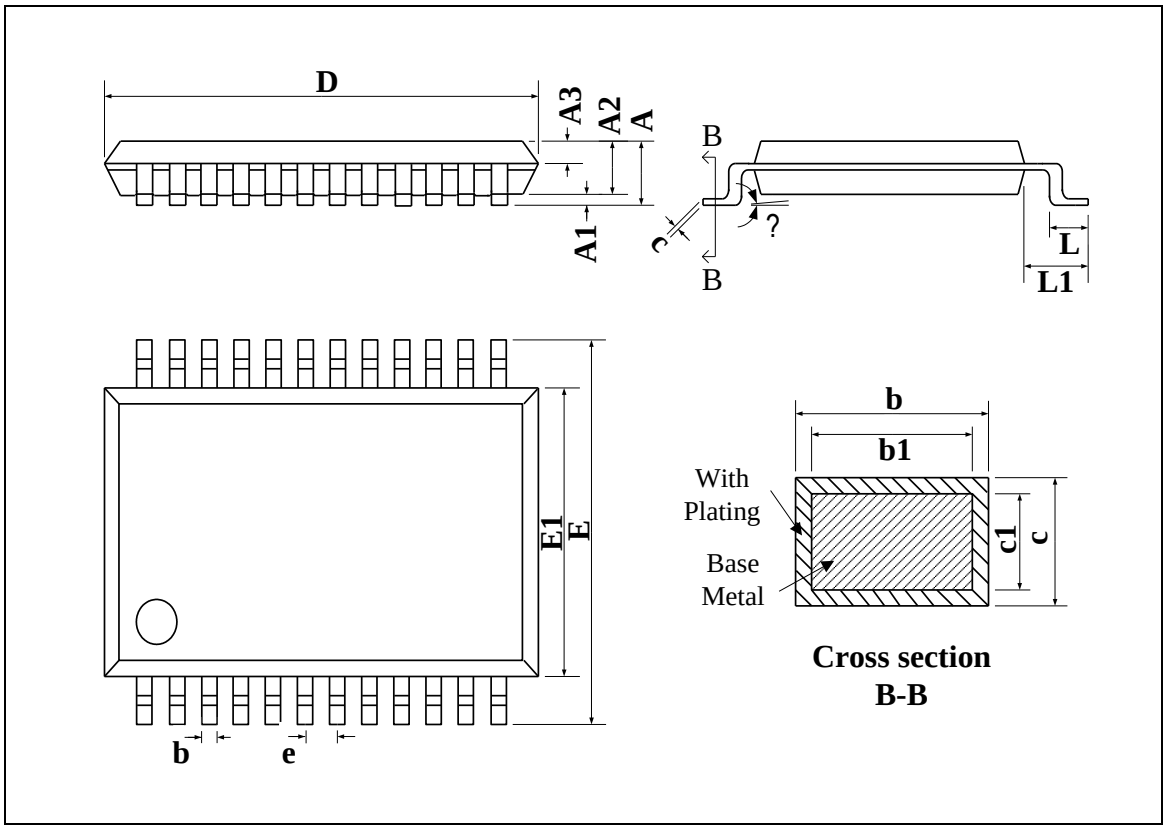
Remarks:
1. CMOS device can easily be damaged by electrostatics. It must be stored in conductive foam, and careful not to exceed the operating voltage range.
2. Turn off power before insert or remove the device.

Table 17. Electrical Specifications（VDD=3.3V, T_A=25℃）

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Remarks
VDD	Power supply	2.0	3.3	3.6	V	Digital circuits operate down to 2.0V
CRYXT	Crystal oscillator frequency	--	32.768	--	kHz	
FOSC	System operating frequency	--	2.097	--	MHz	CRYXT frequency multiplied by PLL
IDD1	Operating current 1		1.2		mA	Normal operation
IDD2	Operating current 2		3		uA	At sleep mode
Fsam	ADC sampling rate	--	1.048	--	MHz	ADC operating frequency
OSR	Over sampling rate	128	--	16384		Can select between 128 to 16384
GAIN	ADC gain	1	--	16		1/2/8/16 selectable
ENOB	Effective number of bits	--	19.5	--	bits	Gain=1
NMbit	No missing code	24	--	--	bits	
INL	Integral nonlinearity	--	0.002	--	%FSR	With external VREF
VINdif	ADC differential input voltage range	-0.6	--	+0.6	V	Gain=1
VINabs	ADC absolute input voltage range	-0.2	--	AVDDR+0.2	V	Gain=1
ACFreq	AC input signal frequency	40	--	400	Hz	0.5% measurement accuracy
Vnrms	RMS noise	--	2.2	--	uVrms	Gain=1
VREF	Voltage reference	--	1.16	--	V	
Rvref	VREF output resistance	--	4	--	kΩ	
TCvref	Vref TC	--	±50	--	ppm/℃	-40℃-85℃
Vavddr	AVDDR output voltage	--	2.4	--	V	SYSTEM [5:4]=00
		--	2.7	--		SYSTEM [5:4]=01
		--	3.0	--		SYSTEM [5:4]=10
		--	3.3	--		SYSTEM [5:4]=11
Iavddr	AVDDR output current	--	10	--	mA	

POR	Power on reset voltage	--	2.0	--	V	
LVD	Low voltage detect threshold	--	1.9	--	V	
THlbt	LVD hysteresis	--	200	--	mV	
Digital I/O parameter						
IOH	High output current source	--	12	--	mA	VOH=VDD-0.3V
IOL	Low output current sink	--	12	--	mA	VOL=0.3V
VOH	Output high voltage	VDD-0.3	--	--	V	
VOL	Output low voltage	--	--	VSS+0.3	V	
Rpu	Pull up resistance	--	200	--	kΩ	VDD = 3.0

Package Information



Dimensions: mm

Symbol	Min.	Nom.	Max.
A	——	——	2.00
A1	0.05	——	0.25
A2	1.65	1.75	1.85
A3	0.75	0.80	0.85
D	8.00	8.20	8.40
E	7.60	7.80	8.00
E1	5.10	5.30	5.50
L	0.75	——	1.05
L1	1.25BSC		
b	0.29	——	0.37
b1	0.28	0.30	0.33
c	0.15	——	0.20
c1	0.14	0.15	0.16
e	0.65BSC		
θ	0°	——	8°

Figure 16. SSOP24 mechanical specification