SD2085
Low Power HART™ Modem

Feature

- Single chip, half duplex 1200 bps FSK modem
- Meets HART physical layer requirements
- Bell 202 shift frequencies of 1200Hz and 2200Hz
- Buffered HART output for drive capability
- Digital signal processing provides reliable input signal detection
- UART interface
- 2.7V to 3.6V power supply
- 85μA maximum supply current in transmit mode
- -55°C to +125°C operation range
- 20pins 5mm x 5mm x 0.75mm TQFN20 package
- RoHS compliant

General Description

The SD2085 is a CMOS single chip modem IC used in Highway Addressable Remote Transducer (HART) field instruments and masters. This IC integrates all necessary filtering, signal detection, modulating, demodulating, and HART signal wave shaping functions. Thus it requires few external passive components to satisfy the HART physical layer requirements.

The SD2085 uses phase continuous Frequency Shift Keying (FSK) at 1200 bps, and operates in half duplex mode per HART protocol. The maximum supply current consumption in transmit mode is 85μA while using 3.6864MHz external Clock source input and 3.6V power supply.

The input HART signal is sampled by an analog to digital converter (ADC), followed by a digital filter and demodulator. This architecture ensures reliable signal detection in noisy environments. A digital to analog converter (DAC) is used to output 1200Hz and 2200Hz phase continuous trapezoid waveforms.

Required board space is very small because of the 5mm x 5mm QFN package and very few external components needed, making it ideal for line-powered applications in both master and slave configurations.

Ordering Information

Package	Part Number
QFN20 5mm x 5mm	SD2085

Pin Diagram and Descriptions

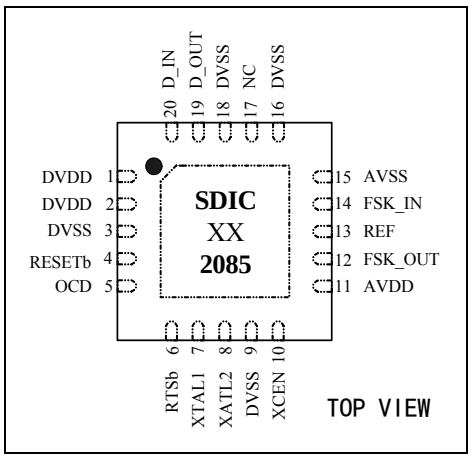


Figure 1. Pin diagram

Table 1. Pin Descriptions

Pin No.	Pin Name	Attribute	Description
1,2	DVDD	Digital power	Digital supply voltage, same voltage level with AVDD.
3, 9, 16, 18	DVSS	Digital gnd	Digital ground, same voltage level with AVSS.
4	RESETb	Digital input	IC reset, active low.
5	OCD	Digital output	Carrier detect. A high state on CD indicates a valid carrier is detected.
6	RTSb	Digital input	Request to send. Low state enables the modulator and disables the demodulator, the IC is in transmit mode. High state enables the demodulator and disables the modulator, the IC is in receive mode.
7	XTAL1	Analog input	Connection for external 3.6864MHz crystal or external clock source input.
8	XTAL2	Analog output	Connection for external 3.6864MHz crystal. Floating when using an external clock source.
10	XCEN	Digital input	Crystal oscillator circuit (XOSC) enable, active low.
11	AVDD	Analog power	Analog supply voltage.
12	FSK_OUT	Analog output	HART FSK signal output. Connect to 4-20mA loop interface circuit.
13	REF	Analog output	Internal 1.5V reference voltage output. Connect a 1μF capacitor to AVSS.
14	FSK_IN	Analog input	FSK modulated HART signal received from 4-20mA loop interface circuit.
15	AVSS	Analog gnd	Analog ground.
17	NC	-	No Connect pin. Can be tied to DVDD or DVSS.
19	D_OUT	Digital output	Demodulated HART data, output to external UART.
20	D_IN	Analog input	Data to be transmitted. After modulation, data goes out at FSK_OUT.
EPAD	AVSS	Analog gnd	Analog ground. For typical application, connect to pin 15.

Circuit Description

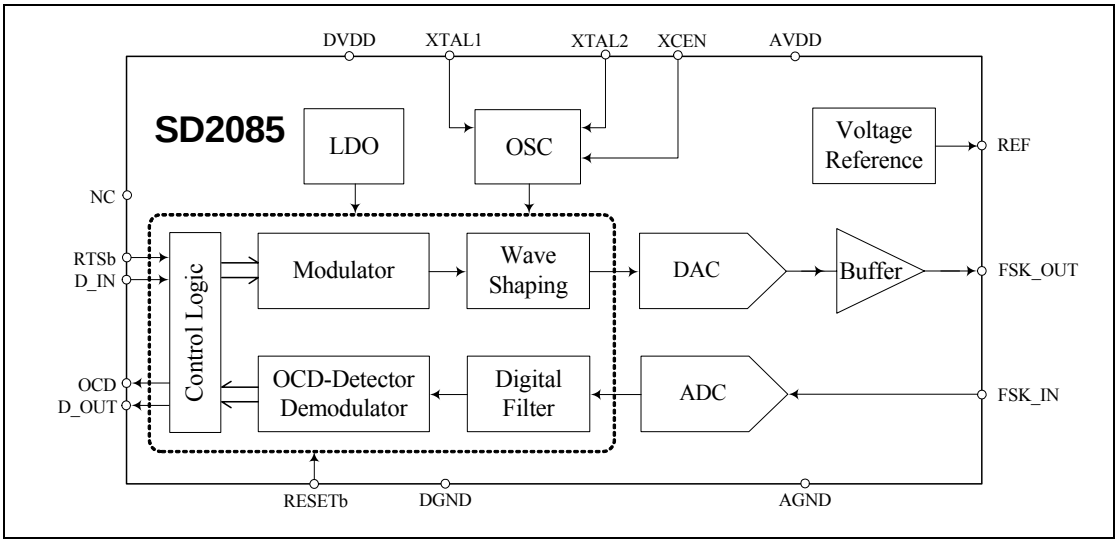


Figure 2. Function block diagram

Figure 2 is the function block diagram of SD2085. It is a low power HART FSK half duplex single chip modem that compiles with HART physical layer requirements. SD2085 includes the modulator, wave shaper, DAC, buffered HART output for transmitting data,

and includes the ADC, digital filter, demodulator, and carrier detect circuitry for receiving data. Other functional blocks include reference voltage, crystal oscillator, and LDO. As a result of such extensive integration, minimal external components are needed. SD2085 is suitable for use in both HART field instrument and master configurations.

The SD2085 either transmits or receives 1200Hz and 2200Hz FSK signals as shown in Figure 3. 1200Hz represents digital "1", whereas 2200Hz represents digital "0". The bit rate is 1200bits/second.

Both crystal oscillator and external clock source are supported.

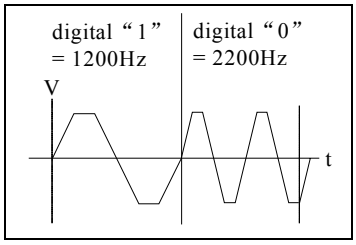


Figure 3. HART FSK signal

FSK Modulator

When RTSb is set to low, the SD2085 operates in transmit mode. The modulator converts the NRZ digital signal at D_IN into a sequence of phase continuous 1200Hz and 2200Hz HART compliant trapezoidal signal through the wave shaping block. The signals are then buffered and output to FSK_OUT. The FSK_OUT DC level is 0.75V with 0.5V~1.0V voltage swing.

The signal going into D_IN is a standard UART frame with 1 start bit, 8 data bits, 1 parity bit, and 1 stop bit as shown in Figure 4.

FSK_OUT can drive capacitive load directly. The load should be 4.7nF to 68nF. SD2085 consumes more current as the capacitive load increases. The supply current specifications shown in Table 3 are based on a 4.7nF capacitive load at FSK_OUT.

If driving a load with resistive element, it should be coupled with a 2.2μF serial capacitor as shown in Figure 5. The R_{LOAD} range is typically 200Ω to 600Ω. A 22nF capacitor should be connected between HART_OUT and ground.

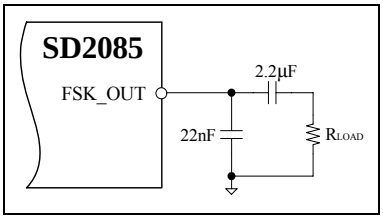


Figure 5. FSK_OUT with resistive load

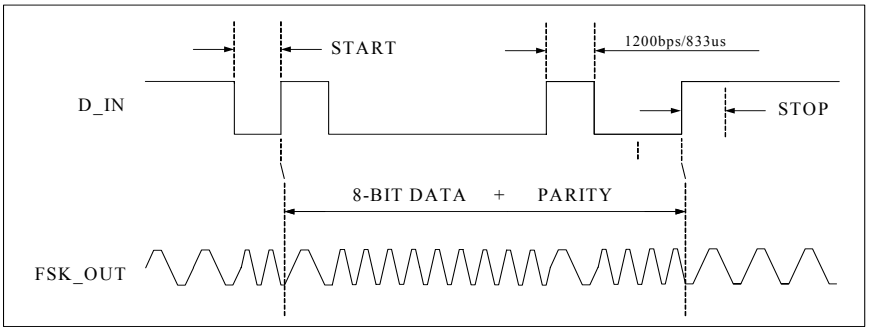


Figure 4. SD2085 Modulator waveform

FSK Demodulator

When RTSb is set to high, the SD2085 operates in receive mode. HART signal goes into FSK_IN through an external anti-aliasing band-pass filter. A high on OCD indicates a valid carrier is detected. The demodulator accepts the FSK signal at FSK_IN and restores to digital signal at D_OUT, which is then output to external UART.

The external band-pass filter is shown in Figure 6. A 200kΩ resistor at the filter input limits current to a sufficiently low level resulting in very high transient voltage protection capability. Therefore, no additional protection circuitry at the input terminal is needed even in the most demanding industrial environments. Using 1% accuracy resistor and 10% accuracy capacitor, effect of the filter on the carrier detection is still negligible.

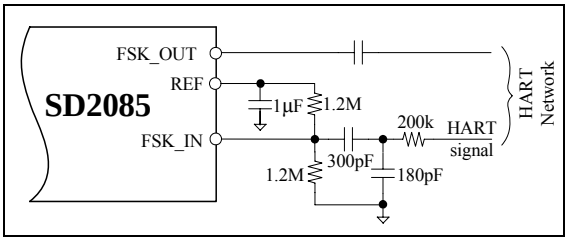


Figure 6. SD2085 external filter connection

The HART bit stream is a standard UART frame with a start bit, 8 data bits, 1 parity, and a stop bit as shown in Figure 7.

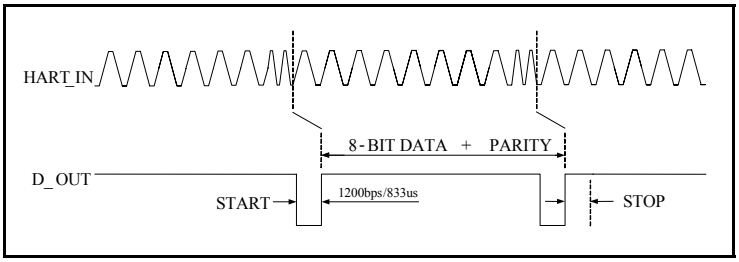


Figure 7. SD2085 Demodulator waveform

Clock Configuration

The SD2085 provides two clocking options: external crystal and CMOS clock input.

The typical connection for the external 3.6864MHz crystal is shown in Figure 8. XCEN is set to low. The crystal and capacitor should be as close to SD2085 as possible.

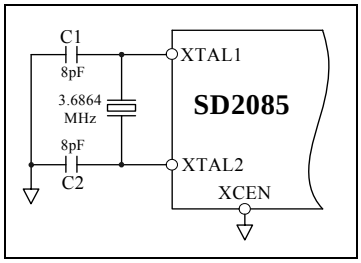


Figure 8. Crystal oscillator connection

The typical connection of CMOS clock input is shown in Figure 9 where an external 3.6864MHz clock source is connected to XTAL1. XTAL2 must be floating. XCEN is set to high.

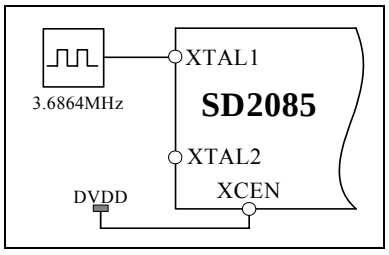


Figure9. CMOS clock connection

Power-Down Mode

When RESETb is at low state, the IC is reset and enters into power down mode. Receive, transmit, and oscillator circuits are all turned off, and the device consumes a maximum of 5μA.

A high state at RESETb returns SD2085 to power-on state. If not using the reset function, one can tie this pin permanently to DVDD.

Using the SD2085

Typical Application Diagram

Figure 10 is a typical smart transducer with HART capability using SD2085 and SD2421 (4-20mA loop-powered DAC). This implementation greatly simplifies system design and enhances reliability while reducing overall PCB size. Decouple the power supplies with 1μF and 0.1μF capacitors in parallel to ground, and decouple the REF pin with a 1μF capacitor to ground.

HART signal comes in from the current loop's LOOP+ terminal, and goes into SD2085's FSK_IN pin through the external band-pass filter. SD2057 demodulates the signal and passes the digital data to the MCU through the D_OUT pin.

To send HART signal out to the current loop, the MCU sends digital data to SD2085's D_IN pin. SD2085 performs modulation and wave shaping, and send the HART signal out through its FSK_OUT pin and the Cc capacitor to SD2421's C3 pin. SD2421 then passes the signal to the current loop.

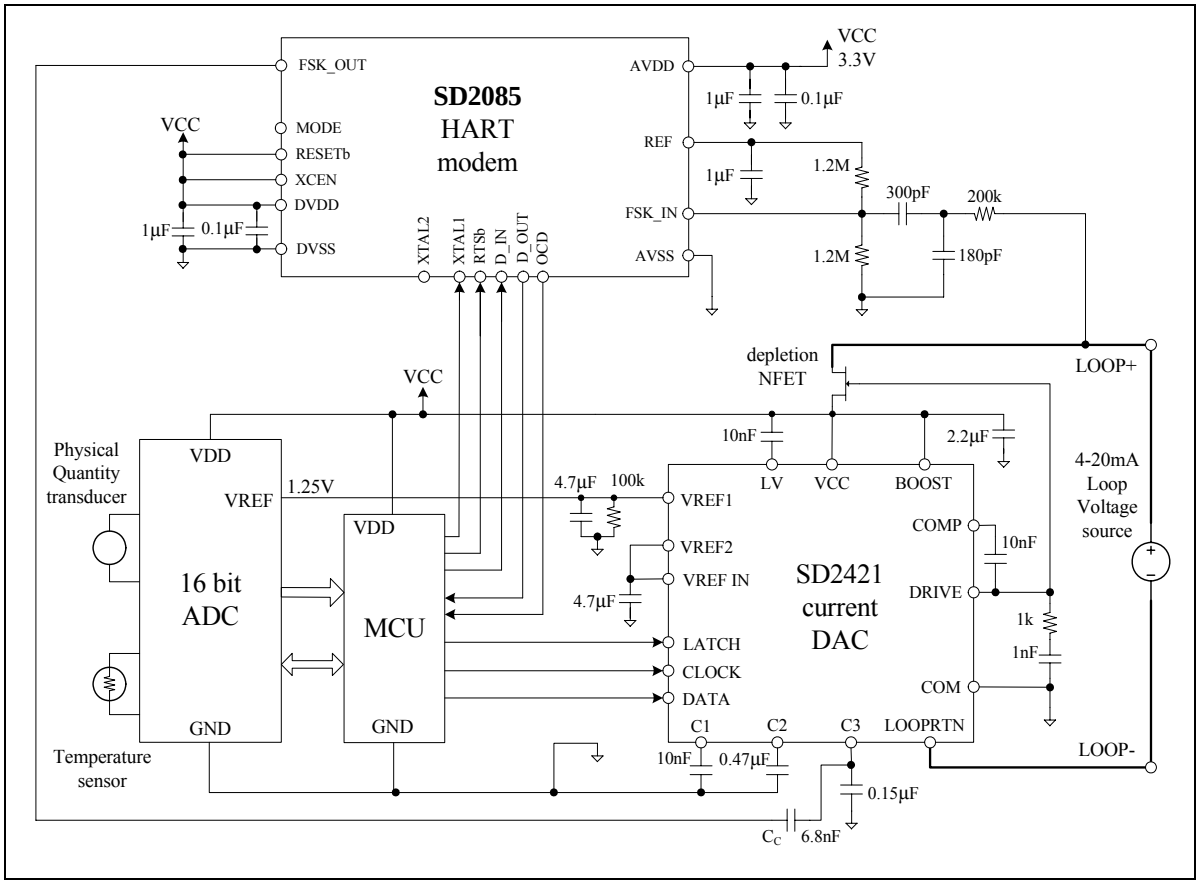


Figure 10. Typical 4-20mA smart transducer with HART digital communication capability

Electrical Specifications

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
T_A	Operating temperature	-55	+125	℃
T_S	Storage temperature	-65	+150	℃
AVDD to AVSS	Analog supply voltage	-0.3	+7.0	V
DVDD to DVSS	Digital supply voltage	-0.3	+7.0	V
AVSS to DVSS	Analog to digital ground	-0.3	+0.3	V
Analog input to AVSS	Analog input/output voltage	-0.3	AVDD+0.3 or +7 (whichever is less)	V
Digital input to DVSS	Digital input/output voltage	-0.3	DVDD+0.3 or +7 (whichever is less)	V
TL	Reflow temperature profile		Per IPC/JEDECJ-STD-020C	℃
ESD	Human body model	4000		V
	Machine model	400		V

Remarks:

1. CMOS device can easily be damaged by electrostatics. It must be stored in conductive foam, and with care taken to not exceed the operating voltage range.
2. Turn off power before inserting or removing the device.

Table 3. Electrical Specifications (AVDD/DVDD=+2.7V~+3.6V, T_A=-55℃~+125℃, AVSS/DVSS=0V, external crystal, 8pF at XTAL1/XTAL2, FSK_OUT with 4.7nF load, unless otherwise noted)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Remarks
AVDD DVDD	Supply voltage	2.7	3.3	3.6	V	
IDD1	ADD+DVDD Demodulator mode		97	125	μA	External clock, -55℃ to +85℃
				130	μA	External clock, -55℃ to +125℃
			125	500		External crystal, -55℃ to +85℃
				550		External crystal, -55℃ to +125℃
	AVDD+DVDD Modulator mode		67	80	μA	External clock, -55℃ to +85℃
				85	μA	External clock, -55℃ to +125℃
			95	450		External crystal, -55℃ to +85℃
				500		External crystal, -55℃ to +125℃
IDD0	Power-down mode		2.5	5	μA	
V_{REF}	Initial accuracy	1.48	1.5	1.52	V	
	Load regulation		1.5		ppm/μA	Tested with 500μA load
	Line regulation		60		μV/V	
OCD assert	Carrier amplitude	90	105	115	mVp-p	
FSK_IN	Input voltage range	0		1.5	V	
FSK_OUT	Output amplitude		500		mVp-p	
	“1” frequency		1200		Hz	
	“0” frequency		2200		Hz	
	Phase error			0	°	
	Maximum resistive load		160		Ω	R_{LOAD} shown in Figure5
External clock	Frequency accuracy	3.6496	3.6864	3.7232	MHz	

Digital I/O parameter						
V_{IH}	Input high voltage	0.7*DVDD			V	
V_{IL}	Input low voltage			0.3*DVDD	V	
I_{IH}	Input high current			±0.1	μA	
I_{IL}	Input low current			±0.1	μA	
t_1	Carrier start time			0.3	Bit time[1]	Time from RTSb falling edge to carrier reaching its first peak. Refer to Figure 11.
t_2	Carrier stop time			1	Bit time[1]	Time from RTSb rising edge to carrier amplitude dropping below the minimum receive amplitude. Refer to Figure 12.
t_3	Carrier decay time			1	Bit time[1]	Time from RTSb rising edge to carrier amplitude dropping to ac zero. Refer to Figure 12.
t_4	Carrier detect on			6	Bit time[1]	Time from carrier on to OCD rising edge. Refer to Figure 13.
t_5	Carrier detect off			6	Bit time[1]	Time from carrier off to OCD falling edge. Refer to Figure 14.

Note:

1. Bit time is the length of time to transfer one bit of data, 1 Bit time = 1/1200Hz = 833.333μs.

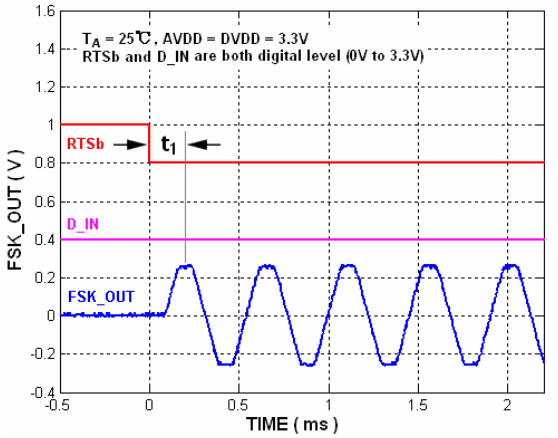


Figure 11. Carrier start time

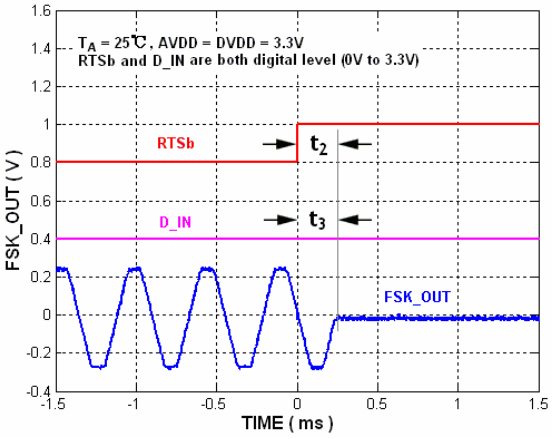


Figure 12. Carrier stop/decay time

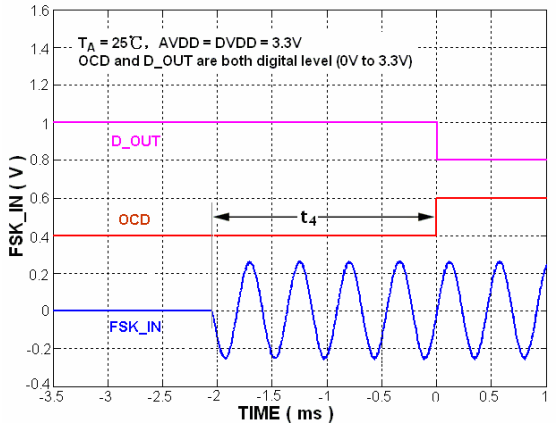


Figure 13. Carrier detect on timing

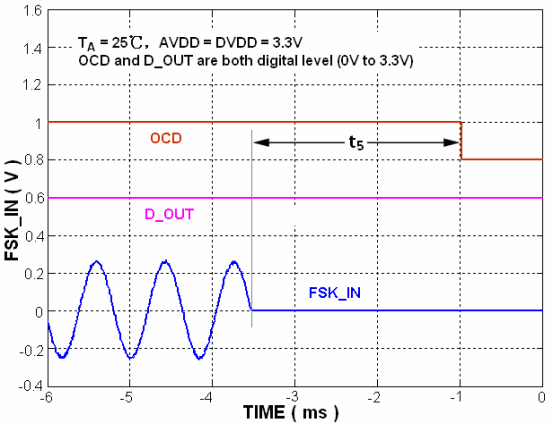
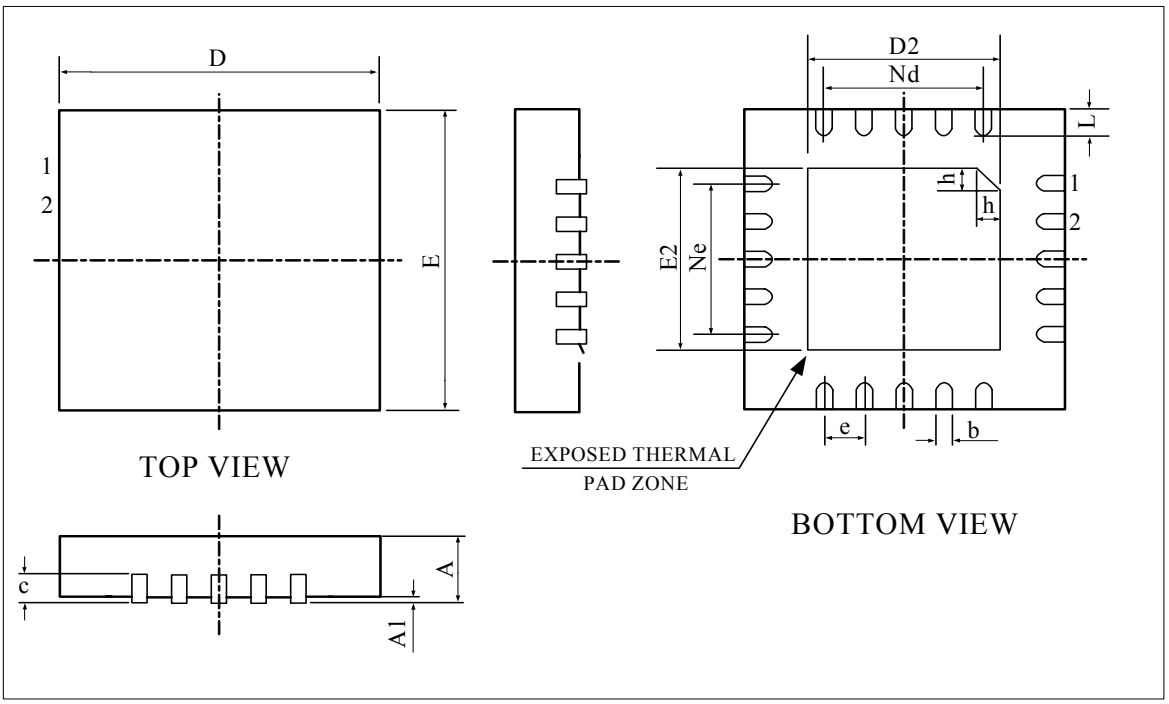


Figure 14. Carrier detect off timing

Packaging Information



Dimension：mm

Symbol	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.25	0.30	0.35
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.05	3.15	3.25
E	4.90	5.00	5.10
E2	3.05	3.15	3.25
e	0.65BSC		
Ne	2.60BSC		
Nd	2.60BSC		
L	0.45	0.55	0.65
h	0.30	0.35	0.40

Figure 15. QFN20 mechanical specification