SD2057
Low Power HART™ Modem

Features

- Meets HART physical layer requirements
- Bell 202 shift frequencies of 1200Hz and 2200Hz
- Integrated receive filter, minimal external components required
- Buffered HART output for drive capability
- UART interface
- 2.7V to 5.5V power supply
- 90μA maximum supply current in transmit mode
- -55°C to +125°C operation range
- 24pins 4mm x 4mm QFN package
- RoHS compliant

General Description

The SD2057 is a CMOS single chip modem IC used in Highway Addressable Remote Transducer (HART) field instruments and masters. This IC integrates all necessary filtering, signal detection, modulating, demodulating, and HART signal wave shaping functions. Thus it requires few external passive components to satisfy the HART physical layer requirements.

The SD2057 uses phase continuous Frequency Shift Keying (FSK) at 1200 bps, and operates in half duplex mode per HART protocol. The maximum supply current consumption in transmit mode is 90μA while using 3.6864MHz external Clock source input and 5.5V power supply.

Required board space is very small because of the 4mm x 4mm QFN package and very few external components needed, making it ideal for line-powered applications in both master and slave configurations.

Ordering Information

Package	Part Number
QFN24 4mm x 4mm	SD2057

Pin Diagram and Descriptions

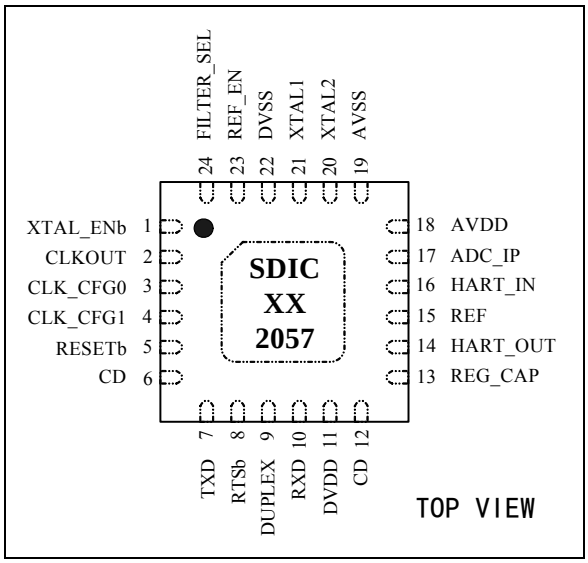


Figure 1. Pin diagram

Table 1. Pin Descriptions

Pin No.	Pin Name	Attribute	Description
1	XTAL_ENb	Digital input	Crystal oscillator circuit (XOSC) enable, active low. Refer to Table 2.
2	CLKOUT	Digital output	Clock output. Refer to “Clock Configuration” section.
3	CLK_CFG0	Digital input	Clock configuration control. Refer to Table 2.
4	CLK_CFG1	Digital input	Clock configuration control. Refer to Table 2.
5	RESETb	Digital input	IC reset, active low.
6	CD	Digital output	Carrier detect, high when a valid carrier is detected at HART_IN.
7	TXD	Digital input	Data to be transmitted. After modulation, data goes out at HART_OUT.
8	RTSb	Digital input	Request to send. Low state enables the modulator and disables the demodulator, the IC is in transmit mode. High state enables the demodulator and disables the modulator, the IC is in receive mode.
9	DUPLEX	Digital input	Full duplex operation enable, active high. Refer to “Full Duplex Operation” section.
10	RXD	Digital output	Demodulated HART data, output to external UART.
11	DVDD	Digital Power	Digital supply voltage, same voltage level with VDDA. Refer to “Supply Decoupling” section.
12	DVSS	Digital gnd	Digital ground, same voltage level with AVSS.
13	REG_CAP	Analog output	Internal voltage regulator output. Connect a 1μF capacitor to DVSS.
14	HART_OUT	Analog output	HART FSK signal output. Connect to 4-20mA loop interface circuit.
15	REF	Analog output	Internal 1.5V reference voltage output or external 2.5V reference voltage input. Connect a 1μF capacitor to AVSS.
16	HART_IN	Analog input	FSK modulated HART signal received from 4-20mA loop interface circuit.
17	ADC_IP	Analog input	If using the internal BPF, connect a 680pF capacitor to this pin. If using the external BPF, the BPF output should connect to this pin directly as shown in Figure 6.
18	AVDD	Analog power	Analog supply voltage. Refer to “Supply Decoupling” section.
19	AVSS	Analog gnd	Analog ground.
20	XTAL2	Analog output	Connection for external 3.6864MHz crystal. Floating when using an external clock source.
21	XTAL1	Analog input	Connection for external 3.6864MHz crystal or external clock source input.
22	DVSS	Digital gnd	Digital interface ground. For typical application, connect this pin to AVSS.
23	REF_EN	Digital input	Reference enable. A high state enables the internal 1.5V reference and buffer. A low state disables the internal reference and buffer. A buffered external 2.5V reference source must then be applied at REF.
24	FILTER_SEL	Digital input	Band pass filter select. A high state enables the internal filter and the HART signal should be applied to the HART_IN pin. A low state disables the internal filter and an external BPF output should be applied to ADC_IP pin.
EPAD	AVSS	Analog gnd	Analog ground. For typical application, connect to pin 19.

Circuit Description

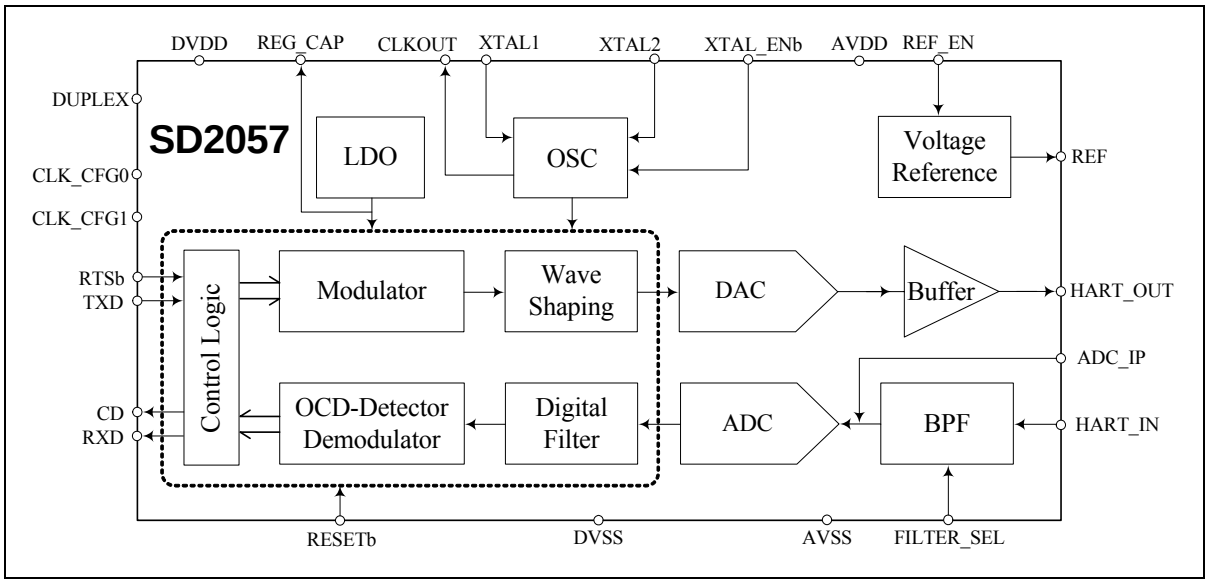


Figure 2. Function block diagram

Figure 2 is the function block diagram of SD2057. It is a low power HART FSK half duplex single chip modem that compiles with HART physical layer requirements. SD2057 includes the modulator, wave shaper, DAC, buffered HART output for transmitting data; and includes the internal band pass filter (can be bypassed if needed), ADC, digital filter, demodulator, and carrier detect circuitry for receiving data. Other functional blocks include reference voltage, crystal oscillator, and LDO. As a result of such extensive integration, minimal external components are needed. SD2057 is suitable for use in both HART field instrument and master configurations.

The SD2057 transmits or receives 1200Hz and 2200Hz FSK signals. 1200Hz represents digital "1", whereas 2200Hz represents digital "0".

Both crystal oscillator and external clock source are supported.

FSK Modulator

When RTSb is set to low, the SD2057 operates in transmit mode. The modulator converts the NRZ digital signals at TXD into a sequence of phase continuous 1200Hz and 2200Hz HART compliant trapezoidal signals through the wave shaping block (see Figure 3). The signals are then buffered and output to HART_OUT. The HART_OUT DC level is 0.75V with 0.5V~1.0V voltage swing.

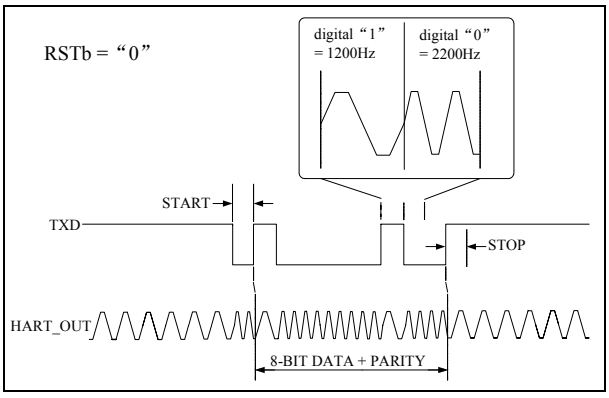


Figure 3. SD2057 modulator waveform

Connecting to HART_OUT

HART_OUT can drive capacitive load directly. The load should be 4.7nF to 68nF, although it can drive larger one. SD2057 consumes more current as the capacitive load increases. Refer to Figure 20 for a typical plot of

supply current vs. capacitive load. The supply current specifications in Table 4 are based on a 4.7nF capacitive load at HART_OUT.

If driving a load with resistive element, it should be coupled with a 2.2μF serial capacitor as shown in Figure 4. The RLOAD range is typically 200Ω to 600Ω. A 22nF capacitor should be connected between HART_OUT and ground.

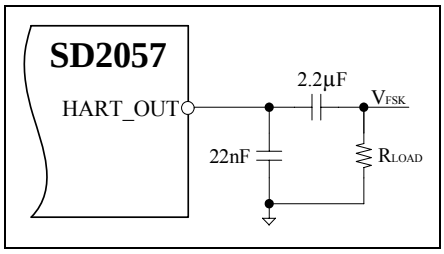


Figure 4. HART_OUT with resistive load

FSK Demodulator

When RTSb is set to high, the SD2057 operates in receive mode. A high on CD indicates a valid carrier at HART_IN is detected. The demodulator accepts the FSK signal at HART_IN and restores to digital signal at RXD, which is then output to external UART. The HART bit stream is a standard UART frame with a start bit, 8 data bits, 1 parity, and a stop bit as shown in Figure 5.

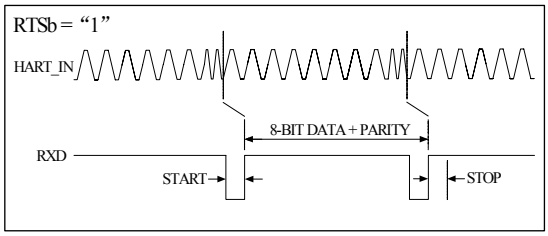


Figure 5. SD2057 demodulator waveform

Connecting to HART_IN or ADC_IP

The SD2057 has two receiving bandpass filter options: an external filter (HART signal is applied to ADC_IP) and an internal filter (HART signal is applied to HART_IN).

When using the external filter, FILTER_SEL should set to 1 and HART_IN should be floating. The configuration is shown in Figure 6 in which the HART signal is applied to ADC_IP through an external anti-aliasing band-pass filter. In safety critical applications, SD2057 must be isolated from the loop's high voltage supply. The recommended external band-pass filter includes a 200kΩ resistor which limits current to a sufficiently low level. The filter input has high transient voltage protection capability and should not require additional protection circuitry even in the most demanding industrial environments. Using 1% accuracy resistor and 10% accuracy capacitor, effect of the filter on the carrier detection is still negligible.

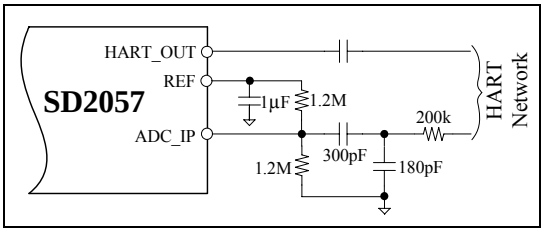


Figure 6. SD2057 using external filter

When using the internal filter, FILTER_SEL should set to 0. The configuration is shown in Figure 7 in which the HART signal is applied to HART_IN through a 2.2nF capacitor. This option is beneficial where cost or board space is of most concern. But mote that it requires extra external protection circuitry for EMC and surge protection if used in harsh industrial environments.

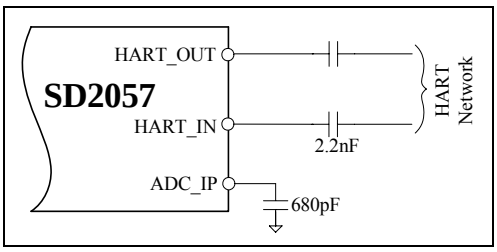


Figure 7. SD2057 using internal filter

Clock Configuration

The SD2057 provides two clocking options: external crystal or CMOS clock input. The various options are configured by CLK_CFG0, CLK_CFG1, and XTAL_ENb as shown in Table 2.

The typical connection for an external 3.6864MHz crystal is shown in Figure 8. The crystal and capacitor should be as close to SD2057 as possible. CLKOUT can be configured to provide a clock output.

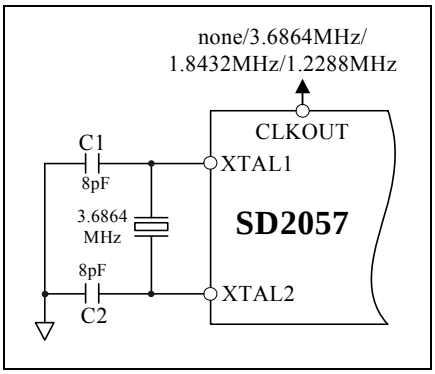


Figure 8. Crystal oscillator connection

The typical connection of CMOS clock input is shown in Figure 9 where an external clock source is connected to XTAL1. XTAL2 must be floating. With this option, CLKOUT cannot provide a clock output.

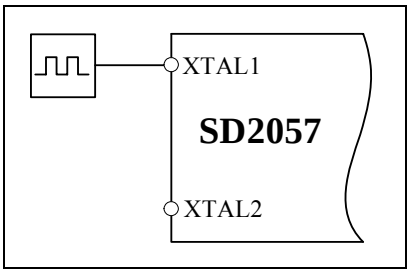


Figure 9. CMOS clock connection

The CLKOUT amplitude is DVDD (V). Enabling CLKOUT increases the device current consumption because the IC has to drive the load at CLKOUT (C). C should be minimized to reduce current consumption and provide the steepest and cleanest clock edges.

The additional current drawn form supply can be calculated using the following equation. *f* is the CLKOUT frequency:

$$I = C \times V \times f$$

Table 2. Clock configuration options

XTAL_ENb	CLK_CFG1	CLK_CFG0	CLKOUT	Description
0	0	0	No output	Crystal oscillator enabled
0	0	1	3.6864MHz output	Crystal oscillator enabled, CLKOUT enabled
0	1	0	1.8432MHz output	Crystal oscillator enabled, CLKOUT enabled
0	1	1	1.2288MHz output	Crystal oscillator enabled, CLKOUT enabled
1	0	0	No output	3.6864 MHz CMOS clock connected at XTAL1 pin
1	0	1	No output	1.2288 MHz CMOS clock connected at XTAL1 pin

Power-Down Mode

When RESETb is at low state, the IC is reset and enters into power down mode. Receive, transmit, and oscillator circuits are all turned off, and the device consumes a maximum of 5μA.

A high state at RESETb returns SD2057 to power-on state. If not using the reset function, one can tie this pin permanently to DVDD.

Full Duplex Operation

As shown in Figure 10, the full duplex mode operation is enabled by setting RTSb to logic low and DUPLEX to logic high. In this mode, SD2057's modulator and demodulator are both enabled. Self-test for the complete signal path between the host controller MCU and the HART device SD2057 can then be ran in order to verify that the local communications loop is functional. The application's safety integrity level (SIL) rating can be improved with such system diagnostics functional.

Using the SD2057

Transient Voltage Protection

Figure 10 shows a HART enabled current input master module with transient voltage protection circuitry, which is very important in harsh industrial control environments. A 10V unidirectional (for protection against positive high voltage transients) transient voltage suppressor (TVS) is placed at the connection points of the current input module. The TVS device must be selected according to the power rating of the specific system. It should have low leakage current. In the event of a transient spike, the 22Ω series resistor limits current into the FSK output pin HART_OUT. The FSK input pin ADC_IP is inherently protected by the 200kΩ resistor, which is part of the external filter circuitry for the FSK input. In addiction, the voltage divider, made up of the 75kΩ and 22kΩ resistors, is used to maintain a 0.75V dc bias at the field side of the FSK output switch.

Figure 11 shows a similar module with two stages protection. The load is outside of the module. A bidirectional (for protection against both positive and negative high voltage transients) TVS is used at the connection points, which makes the module input polarity more flexible. Because this module could be connected at any point along the current loop, a higher TVS rating was chosen. In addition, the TVS at the field side of the FSK output switch provides secondary protection for SD2057. It can have a lower power rating.

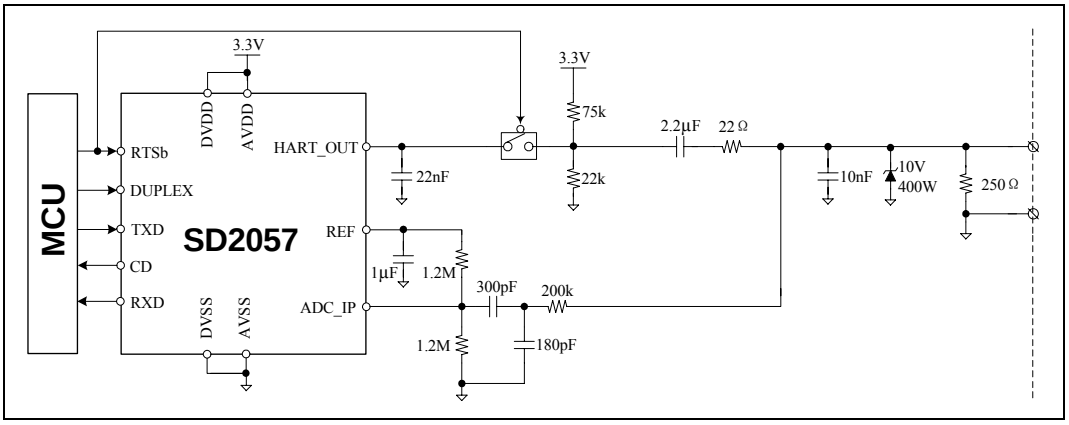


Figure 10. Current input module with HART function enabled (Master)

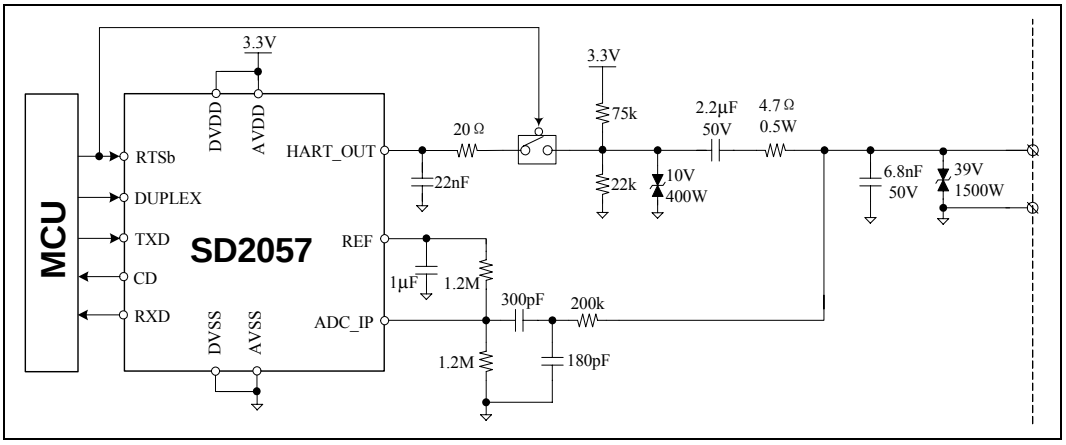


Figure 11. Two-stage protection for HART device (Master)

Supply Decoupling

AVDD and DVDD supplies should both be decoupled to ground with low ESR 1μF in parallel with 0.1μF capacitors.

SD2057 has an internal 2V fast transient response LDO regulator providing power to its digital circuitry. The output is at REG_CAP. It should be decoupled to ground with a 1μF ceramic capacitor. A similar capacitor should be used between REF and ground. Place decoupling capacitors as close to the relevant pins as possible.

Typical Application Diagram

Figure 12 is a typical smart transducer with HART capability using SD2057 and SD2421 (4-20mA loop-powered DAC). This implementation greatly simplifies system design and enhances reliability while reducing overall PCB size.

HART signal comes in from the current loop's LOOP+ terminal, and goes into SD2057's ADC_IP pin through the external band-pass filter. SD2057 demodulates the signal and passes the digital data to the MCU through the RXD pin.

To send HART signal out to the current loop, the MCU sends digital data to SD2057's TXD pin. SD2057 performs modulation and wave shaping, and send the HART signal out through its HART_OUT pin and the Cc capacitor to SD2421's C3 pin. SD2421 then passes the signal to the current loop.

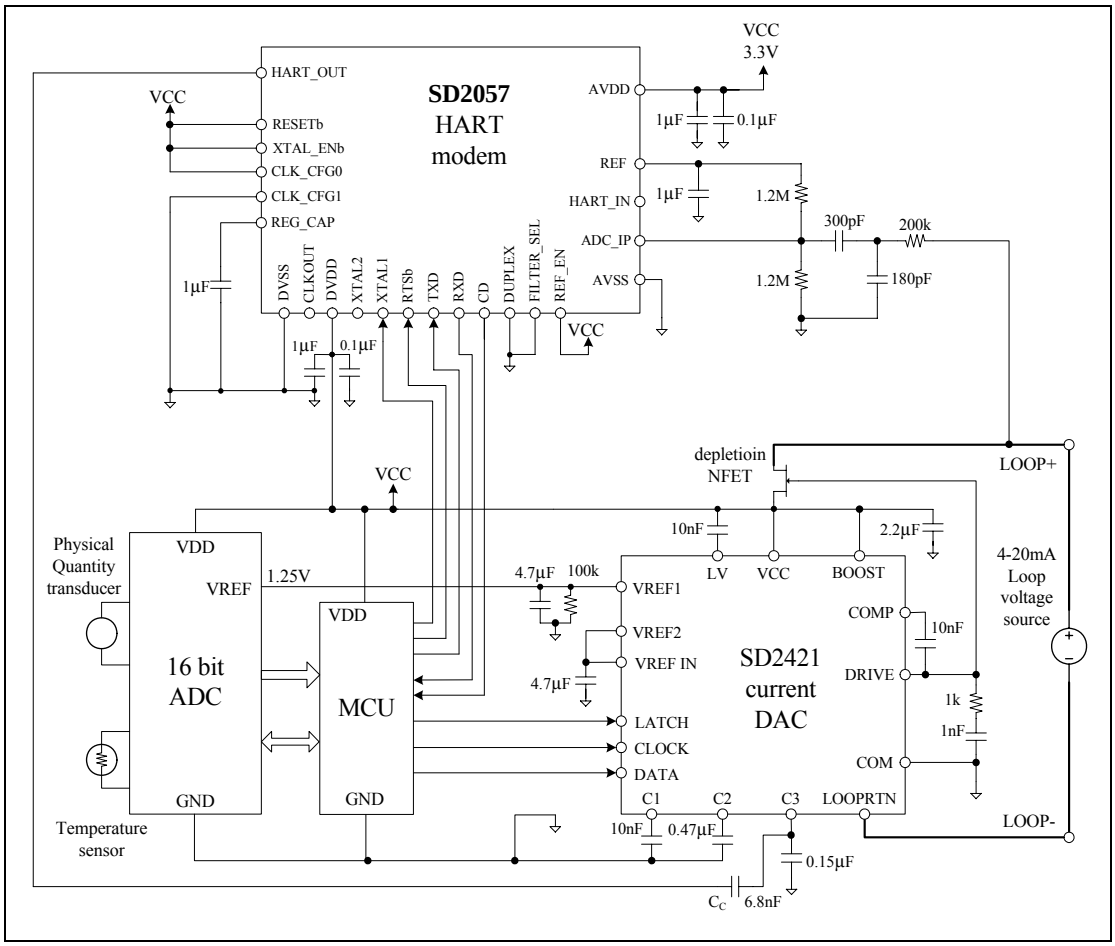


Figure 12. Typical 4-20mA smart transducer with HART digital communication capability

Electrical Specifications

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
T_A	Operating temperature	-55	+125	℃
T_S	Storage temperature	-65	+150	℃
AVDD to AVSS	Analog supply voltage	-0.3	+7.0	V
DVDD to DVSS	Digital supply voltage	-0.3	+7.0	V
AVSS to DVSS	Analog to digital ground	-0.3	+0.3	V
Analog input to AVSS	Analog input/output voltage	-0.3	AVDD+0.3 or +7 (whichever is less)	V
Digital input to DVSS	Digital input/output voltage	-0.3	DVDD+0.3 or +7 (whichever is less)	V
TL	Reflow temperature profile		Per IPC/JEDECJ-STD-020C	℃
ESD	Human body model	4000		V
	Machine model	400		V

Remarks:

1. CMOS device can easily be damaged by electrostatics. It must be stored in conductive foam, and with care taken to not exceed the operating voltage range.
2. Turn off power before inserting or removing the device.

Table 4. Electrical Specifications (AVDD/DVDD=+2.7V~+5.5V, T_A=-55℃~+125℃, AVSS/DVSS=0V, External 3.6864MHz clock source, CLKOUT disabled, HART_OUT with 4.7nF load, internal and external receive filter, internal voltage reference, unless otherwise noted)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Remarks
AVDD DVDD	Supply voltage	2.7	3.3	5.5	V	
IDD1	AVDD+DVDD Demodulator mode		97	135	μA	External clock, -55℃ to +85℃
				140	μA	External clock, -55℃ to +125℃
			77	107	μA	External clock, -55℃ to +85℃, external reference
				113	μA	External clock, -55℃ to +125℃, external reference
	AVDD+DVDD Modulator mode		67	85	μA	External clock, -55℃ to +85℃
				90	μA	External clock, -55℃ to +125℃
			47	65	μA	External clock, -55℃ to +85℃, external reference
				70	μA	External clock, -55℃ to +125℃, external reference
IDD0	Power-down mode		2.5	5	μA	
I_{OSC}	Crystal OSC		45	90	μA	External crystal, 8pF at XTAL1/2
Internal V_{REF}	Initial accuracy	1.48	1.5	1.52	V	REF_EN=DVDD
	Load regulation		1.5		ppm/μA	Tested with 500μA load
	Line regulation		60		μV/V	
External V_{REF}	Initial accuracy	2.47	2.5	2.53	V	REF_EN=DVSS
I_{REF}	External V_{REF} Input current		3.4	5	μA	Demodulator mode
			2.7	4	μA	Modulator mode
REG_ CAP						
CD assert	Carrier amplitude	90	105	115	mVp-p	

HART_IN	Input voltage range	0		REF	V	Using external reference source
		0		1.5	V	Using internal reference source
HART_OUT	Output amplitude	460	500	505	mVp-p	V_{FSK}, as shown in Figure 4
	"1" frequency		1200		Hz	
	"0" frequency		2200		Hz	
	Phase error			0	°	
	Maximum resistive load		160		Ω	R_{LOAD} shown in Figure 4
	Transmit impedance		17		Ω	RTSb low, at the HART_OUT pin
			17		Ω	RTSb high, at the HART_OUT pin
External clock	Frequency accuracy	3.6496	3.6864	3.7232	MHz	External 3.6864MHz clock input
		1.2165	1.2288	1.2411	MHz	External 1.2288MHz clock input
Digital I/O parameter						
V_{IH}	Input high voltage	0.7*DVDD			V	
V_{IL}	Input low voltage			0.3*DVDD	V	
I_{IH}	Input high current			±0.1	μA	
I_{IL}	Input low current			±0.1	μA	
t_1	Carrier start time			1	Bit time[1]	Time from RTSb falling edge to carrier reaching its first peak. Refer to Figure 13.
t_2	Carrier stop time			1	Bit time[1]	Time from RTSb rising edge to carrier amplitude dropping below the minimum receive amplitude. Refer to Figure 14.
t_3	Carrier decay time			1	Bit time[1]	Time from RTSb rising edge to carrier amplitude dropping to ac zero. Refer to Figure 14.
t_4	Carrier detect on			6	Bit time[1]	Time from carrier on to CD rising edge. Refer to Figure 15.
t_5	Carrier detect off			6	Bit time[1]	Time from carrier off to CD falling edge. Refer to Figure 16.
t_6	Crystal OSC power-up time		24.5		ms	8pF at XTAL1 and XTAL2.
t_7	REF reference power-up time		0.5		ms	Internal reference voltage source.
t_8	Wake-up time		18		μs	Transition time from Power-Down Mode to normal operating mode (external clock source, external reference voltage source).

Note:

1. Bit time is the length of time to transfer one bit of data, 1 Bit time = 1/1200Hz = 833.333μs.

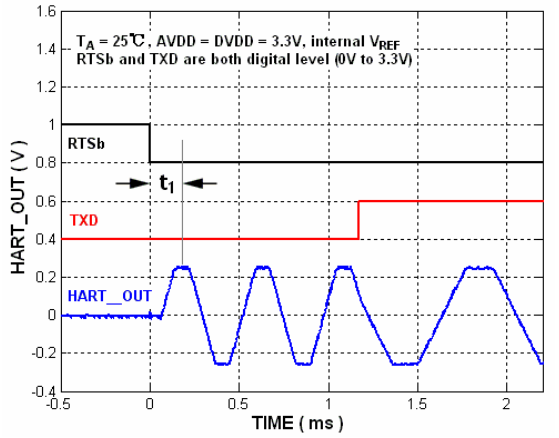


Figure 13. Carrier start time

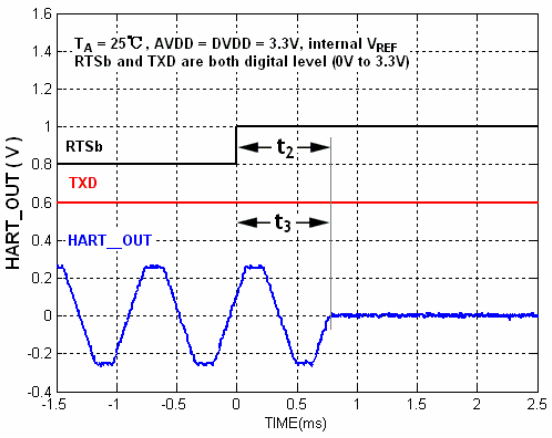


Figure 14. Carrier stop/decay time

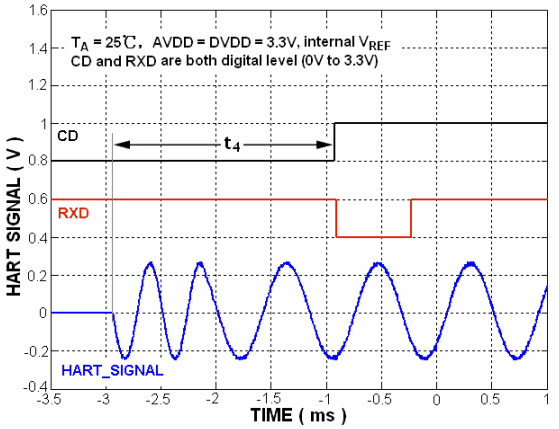


Figure 15. Carrier detect on timing

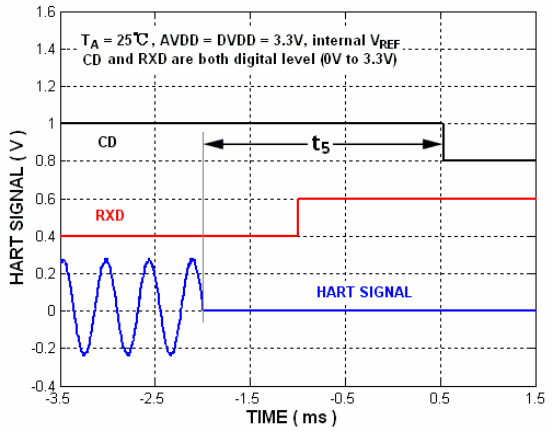


Figure 16. Carrier detect off timing

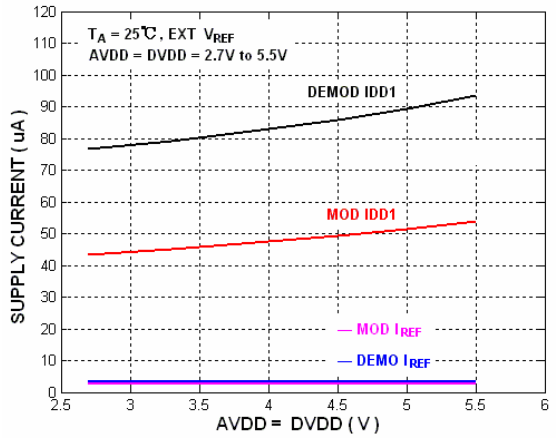


Figure 17. Supply current vs. supply voltage @ external reference

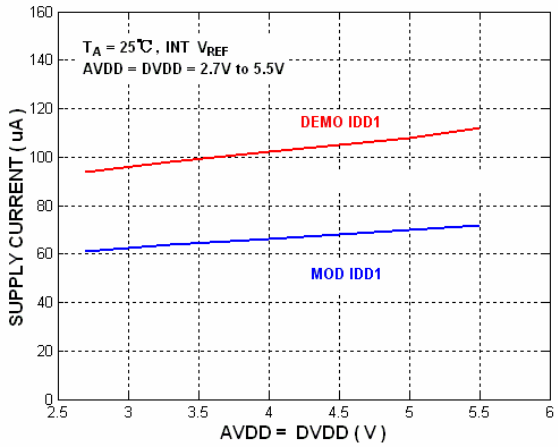


Figure 17. Supply current vs. supply voltage @ internal reference

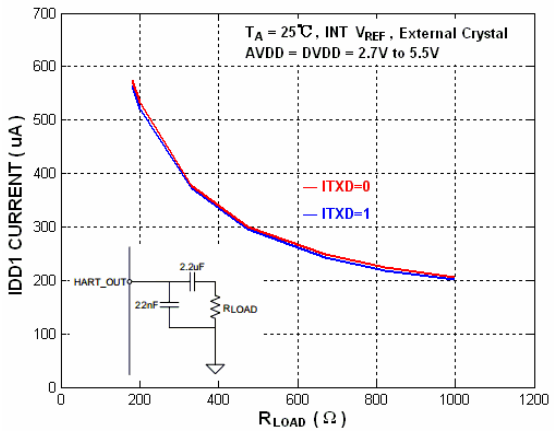


Figure 19. Supply current in transmit mode vs. resistive load

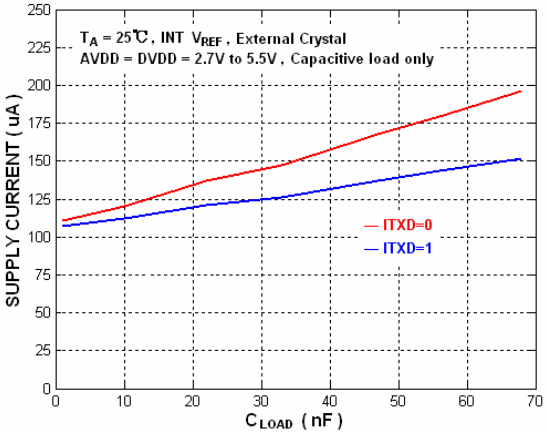


Figure 20. Supply current in transmit mode vs. capacitive load

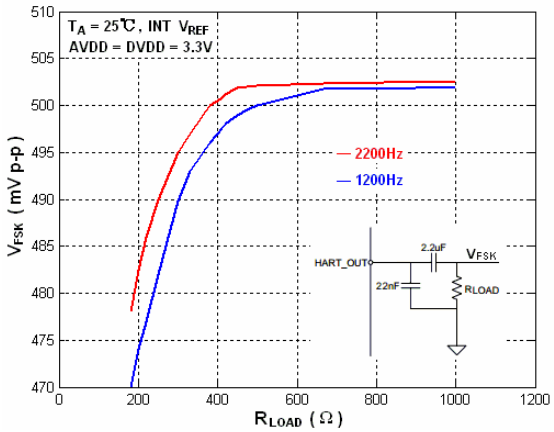


Figure 21. HART output amplitude vs. resistive load

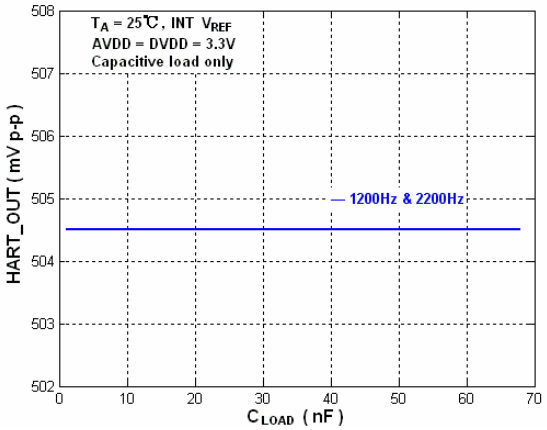


Figure 22. HART_OUT amplitude vs. capacitive load

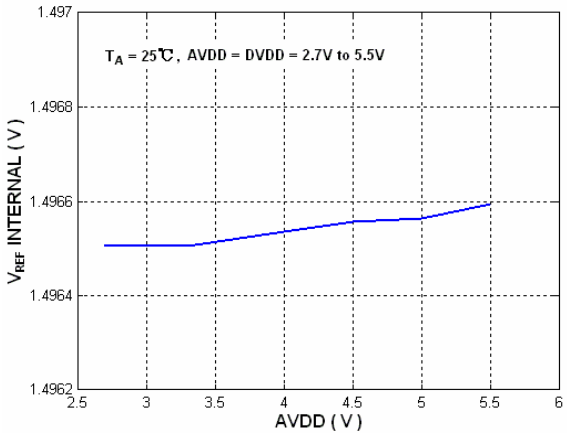


Figure 23. REF reference voltage vs.AVDD

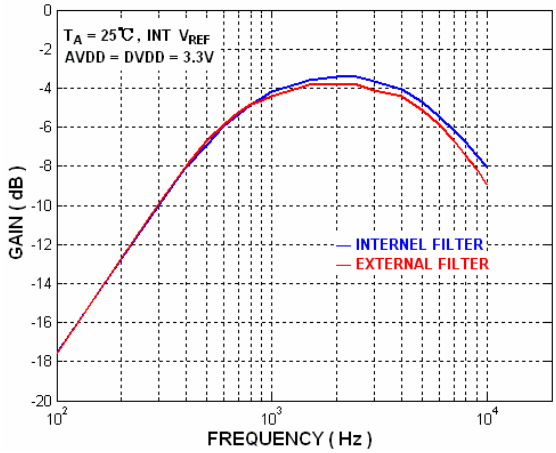
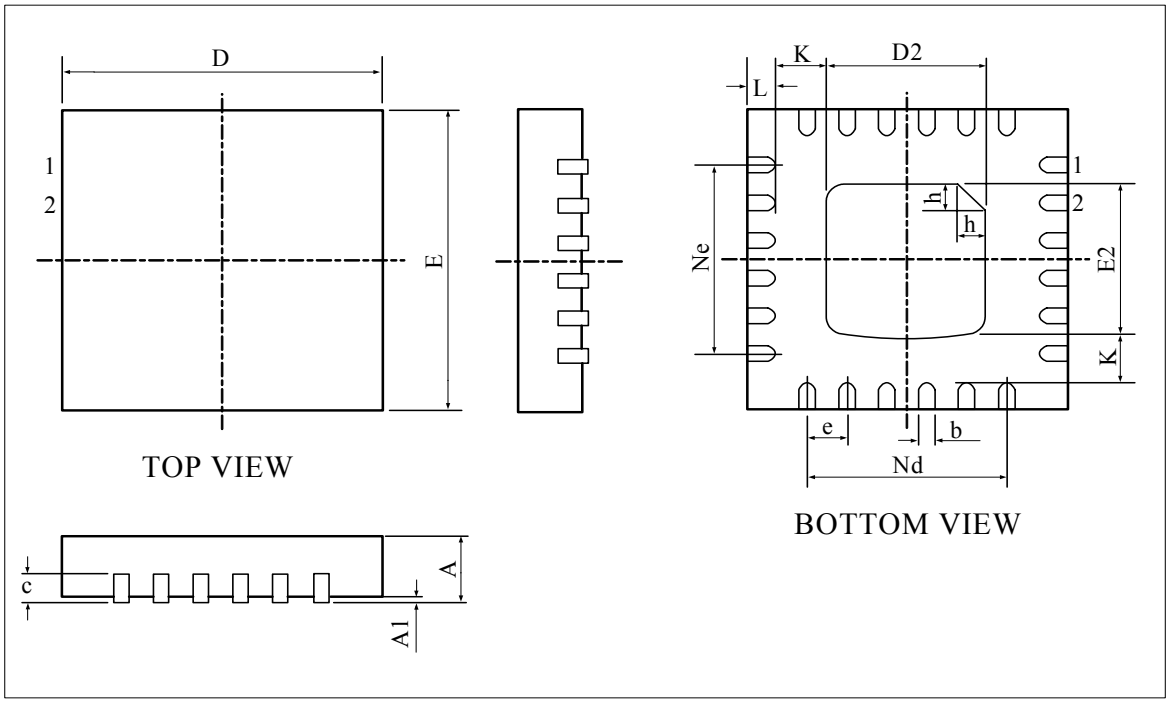


Figure 24. Input BPF frequency response

Packaging Information



Dimension：mm

Symbol	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	1.90	2.00	2.10
E	3.90	4.00	4.10
E2	1.90	2.00	2.10
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
L	0.30	0.40	0.50
K	0.20	—	—
h	0.30	0.35	0.40

Figure 25. QFN24 mechanical specification