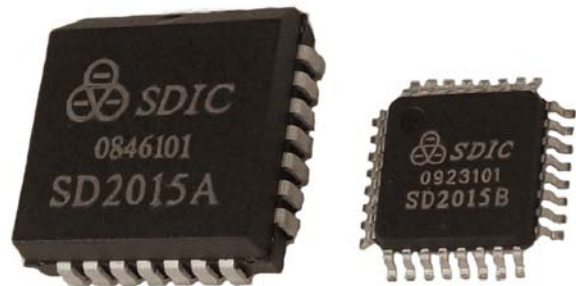


1.0 Feature

- Meets HART physical layer requirements
- Can be used in designs presently using HT2015, A5191HRT, or equivalent type chips
- Lowest current consumption among existing equivalent chips
- Bit Error Rate (BER) typically lower than 1ppm
- 3.0V - 5.5V power supply
- Single chip, half duplex 1200 bps FSK modem
- Bell 202 shift frequencies of 1200Hz and 2200Hz
- Transmit signal wave shaping and receive band pass filter
- Internal oscillator requires 460.8kHz crystal or ceramic resonator
- Industrial temperature range of -40°C to +85°C
- Available in 28 pin PLCC and 32 pin LQFP packages
- RoHS compliant

one hundred times lower than the HART requirement. Both SD2015A (28 pin PLCC) and SD2015B (32 pin LQFP) are RoHS compliant. The SD2015 is 100% pin compatible with HT2015 or A5191HRT. No component needs to be changed when replacing A5191HRT. One component needs to be changed (Figure 8, R6) when replacing HT2015.



2.0 Description

The SD2015 is a CMOS single chip modem IC used in Highway Addressable Remote Transducer (HART) field instruments and masters. This IC together with a few external passive components provide all functions needed to satisfy HART physical layer requirements including modulation, demodulation, receive filtering, carrier detect, and transmit signal wave shaping. See the Pin Descriptions and Functional Description sections for details.

The SD2015 uses phase continuous Frequency Shift Keying (FSK) at 1200 bps, and operates in half duplex mode per HART protocol. Typical current consumption at 25°C ambient is 250µA at 5V and 150µA at 3.3V. Typical BER is less than 1ppm. It is

3.0 Ordering Information

The SD2015 is available in 28 pin Plastic Leaded Chip Carrier (PLCC) and 32 pin Low profile Quad Flat Pack (LQFP). Use the part number in Table 1 when ordering.

Package	Part Name
28 pin PLCC	SD2015A
32 pin LQFP	SD2015B

Table 1. Ordering Information

4.0 Pin Descriptions

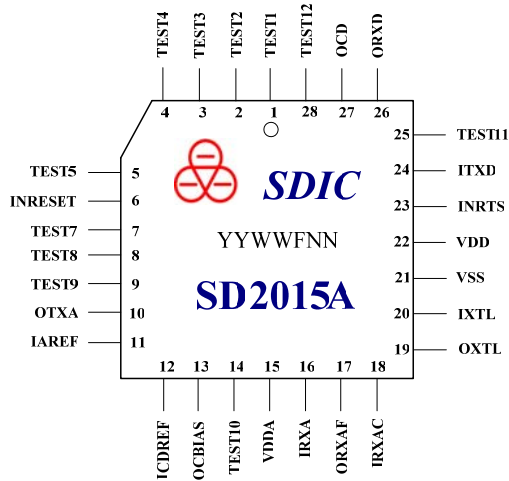


Figure 1. 28 Pin PLCC pin out diagram

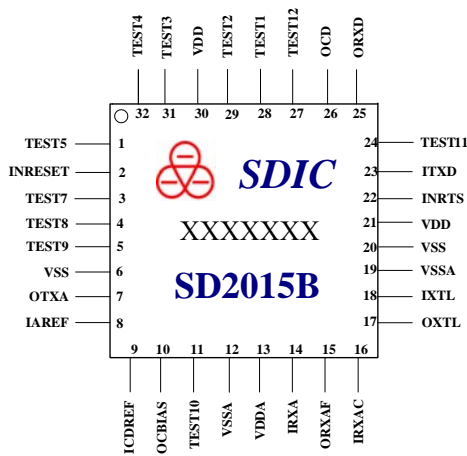


Figure 2. 32 Pin LQFP pin out diagram

Table 2. Pin Descriptions

Signal Name	Type	PLCC	LQFP	Pin Description
TEST1	-	1	28	No Connect or connect to VSS ¹
TEST2	-	2	29	No Connect
TEST3	-	3	31	No Connect
TEST4	-	4	32	No Connect
TEST5	-	5	1	No Connect or connect to VSS
INRESET	Input	6	2	Reset all digital logic, active low
TEST7	Input	7	3	Connect to VSS
TEST8	Input	8	4	Connect to VSS
TEST9	Input	9	5	Connect to VSS
OTXA	Output	10	7	Analog FSK modulated HART transmit signal send to 4-20mA loop interface
IAREF	Input	11	8	Analog reference voltage
ICDREF	Input	12	9	Carrier detect reference voltage
OCBIAS	Output	13	10	Circuit bias current
TEST10	-	14	11	No Connect or connect to VSS
VDDA	Power	15	13	Analog supply voltage, at same level with VDD
IRXA	Input	16	14	FSK modulated HART receive signal from 4-20mA loop interface circuit
ORXAF	Output	17	15	Analog receive filter output
IRXAC	Input	18	16	Analog receive comparator input
OXTL	Output	19	17	Crystal oscillator output
IXTL	Input	20	18	Crystal oscillator input
VSS	Ground	21	6,20	Ground
VDD	Power	22	21,30	Digital supply voltage, same level with VDDA
INRTS	Input	23	22	Request to sent, active low
ITXD	Input	24	23	Digital HART data stream from UART, to be transmit out through OTXA
TEST11	-	25	24	No Connect
ORXD	Output	26	25	Received HART data stream through IRXA, demodulated and send to UART
OCD	Output	27	26	Carrier detect output, high when data valid at IRXA
TEST12	-	28	27	No Connect
VSSA	Ground	-	12,19	Analog ground

1. No connection inside IC. Pin can be connected to VSS for backward compatibility.

IAREF: Analog Reference Voltage

This analog input sets the dc operating point of the operational amplifiers and comparators. See Table 4 for appropriate voltage levels.

ICDREF: Carrier Detect Reference Voltage

This analog input controls the threshold level beyond which the carrier detect (OCD) becomes active. This is determined by the DC voltage difference between IAREF and ICDREF. Selecting $IAREF - ICDREF$ to $80mV_{DC}$ will set the carrier detect threshold to a nominal $100mV_{p-p}$.

INRESET: Reset Digital Logic

When at logic low this input resets all digital logic. It should be held low for a minimum of 10ns after V_{DD} passes 2.5V as shown in Figure 3.

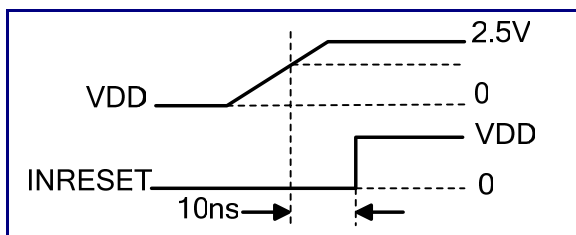


Figure 3. Reset timing

INRTS: Request To Send

This active low input asks the SD2015 to start the transmit operation. OTXA is enabled when this signal is low. This signal must be held high during power up.

IRXA: Analog Receive Input

This is the amplifier input of the receiver high pass filter. It accepts the 1200/2200Hz FSK HART signals from the 4-20mA loop as shown in Figure 8.

IRXAC: Analog Receive Comparator Input

This is the positive input of the receiver filter comparator and the carrier detect comparator.

ITXD: Digital Transmit Input

This input to the modulator accepts digital HART

data in NRZ form. When ITXD is low (logic 0), the modulator output frequency at OTXA is 2200Hz. When ITXD is high (logic 1), the modulator output frequency is 1200Hz.

IXTL: Oscillator Input

This input to the internal oscillator must be connected to a parallel mode 460.8kHz crystal oscillator or ceramic resonator when using the internal oscillator circuit. It should be grounded when using an external 460.8kHz clock signal. See Figure 9 and Figure 10 for connection details.

OCBIAS: Circuit Bias Current

The current through this output controls the bias current of several functional blocks. This current should be set to approximately $2.5\mu A$.

OCD: Carrier Detect Output

This output goes high when a valid data signal input is recognized on IRXA. Valid input is defined as four or more continuously receiving HART data that are greater than the threshold set by IAREF and ICDREF.

ORXAF: Analog Receive Filter Output

This is the amplifier output of the receiver high-pass filter as shown in Figure 8.

ORXD: Digital Receive Output

This digital output is the demodulated HART data signal received through IRXA. When IRXA is 1200Hz, ORXD outputs logic 1. When IRXA is 2200Hz, ORXD outputs logic 0. ORXD is qualified internally with OCD and is logic 1 when OCD is logic 0.

OTXA: Analog Transmit Output

This pin outputs the trapezoidal signal controlled by ITXD. When ITXD is logic 0, the output frequency is 2200Hz. When ITXD is logic 1, the output frequency is 1200Hz. This output is active

when INRTS is logic 0. See Table 5 for detail specifications.

OXTL: Oscillator Output

This is the internal oscillator output. It can also be used as the input port for an external 460.8kHz clock source. See Figure 9 and Figure 10 for connection details.

TEST (1:12): Factory Test

These are factory test pins. For normal operation, tie these pins as shown in Table 2.

VDD: Digital Supply Voltage

This is the power for the digital circuitry.

VDDA: Analog Supply Voltage

This is the power for the analog circuitry.

VSS: Ground

This is the digital ground in LQFP 32 package. It is both digital and analog ground in the PLCC 28 package.

VSSA: Analog Ground

This is the analog ground.

5.0 Function Description

The SD2015 is a functional equivalent of the HT2015 or A5191HRT modem IC. It contains a transmit data modulator, signal shaper, analog receiver filter, demodulator, carrier detect circuitry, and an oscillator. A functional block diagram is shown in Figure 4.

The internal HART modem modulates the transmit signal and demodulates the receive signal. The transmit signal shaper enables the SD2015 to transmit a HART compliant signal. The carrier is detected by comparing the receiver filter output with the difference between two external voltage references IAREF and ICDREF. The received signal goes through a band pass filter before entering the demodulator and the carrier detect circuitry. The oscillator provides the modem with a stable time base using either a simple external resonator or an external clock source.

The modem implements FSK format with logic 0 at 2200Hz and logic 1 at 1200Hz. The bit rate is 1200 bits/second.

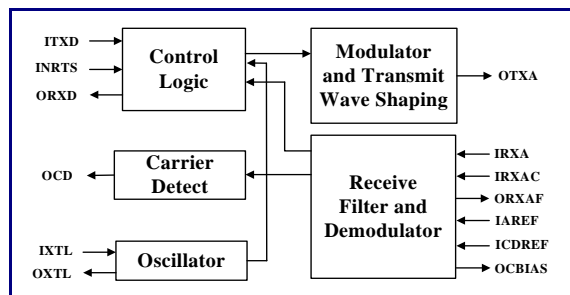


Figure 4. SD2015 block diagram

5.1 Modulator and Transmit Wave Shaping

The modulator accepts digital data in NRZ form at the ITXD input and generates the FSK modulated signal. The transmit signal shaper generates a HART compliant signal at OTXA as shown in

Figure 5 and Figure 6. INRTS must be at logic 0 for the modulator to be active.

For $IAREF = 1.235V_{DC}$, OTXA will have a voltage swing from approximately 0.25 to 0.75V. For $IAREF = 2.5V_{DC}$, OTXA will have a voltage swing from approximately 0.5 to 1.5V.

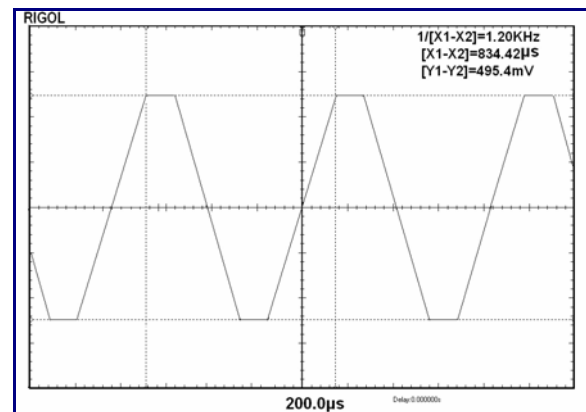


Figure 5. OTXA waveform at logic 1 (1200Hz)

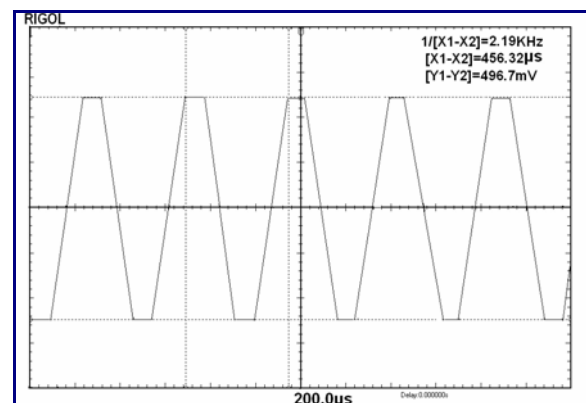


Figure 6. OTXA waveform at logic 0 (2200Hz)

5.2 Demodulator and Carrier Detect

The demodulator accepts a FSK signal at the IRXA input and reproduces the original data signal at the ORXD output. The nominal bit rate is 1200 bps. Figure 7 illustrates the demodulation process.

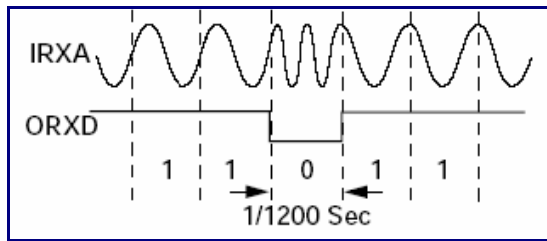


Figure 7. Demodulator signal timing

The output of the demodulator is qualified with OCD. Only those IRXA signals large enough to be detected (100mVp-p typically) by the carrier detect circuit can produce received serial data at ORXD. Maximum demodulator jitter is 12 percent of one bit given input frequencies within HART specifications, a clock frequency of 460.8kHz (± 1.0 percent), and zero input (IRXA) asymmetry.

The carrier detect comparator and the carrier detect block (see Figure 4 and Figure 8) together set the carrier detect output pin OCD to logic 1 if INRTS is logic 1 and four consecutive pulses out of the comparator have arrived. OCD stays logic 1 as long as INRTS is logic 1 and the next comparator pulse is received in less than 2.5ms. Once OCD goes inactive (logic 0), it takes another four consecutive pulses out of the comparator to assert OCD again. Four consecutive pulses amount to 3.33ms when the received signal is 1200Hz, and to 1.82 ms when the received signal is 2200Hz.

5.3 Analog Receiver Circuitry

5.3.1 Voltage References

The SD2015 requires two voltage references IAREF and ICDREF. IAREF sets the dc operating point of the internal operational amplifiers and comparators. See Table 4 for appropriate IAREF values. The level at which OCD becomes active is determined by the dc voltage difference (IAREF - ICDREF). A voltage difference of 80mV will set the carrier detect threshold to a nominal 100mVp-p.

5.3.2 Bias Current Resistor

The SD2015 requires a bias current resistor R_{BIAS} to be connected between OCBIAS and VSS. The bias current controls the operating point of several internal functional blocks. It should be set to approximately 2.5 μ A. The recommended R_{BIAS} value is 500K Ω when IAREF is 1.235V, and 1M Ω when IAREF is 2.5V.

In Figure 8 all external capacitor values have a tolerance of $\pm 5\%$ and the resistors have a tolerance of $\pm 1\%$, except the 3M Ω which has a tolerance of $\pm 5\%$. External to the SD2015, the filter exhibits a three-pole, high-pass filter at 624Hz and a one-pole, low-pass filter at 2500Hz. Internally, the SD2015 has a high-pass pole at 35 Hz and a low-pass pole at 109kHz. The low-pass pole can vary as much as ± 30 percent. The input impedance of the entire filter is greater than 6.7M Ω , at frequencies below 50Hz.

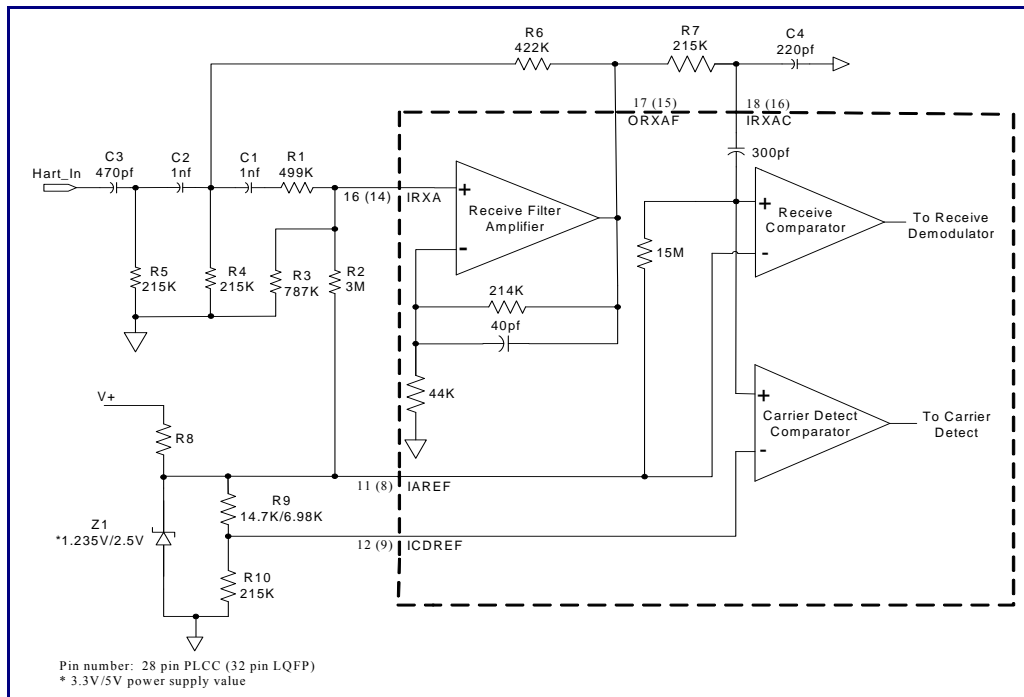


Figure 8. Receive filter schematic

5.4 Oscillator

The SD2015 requires a 460.8kHz clock signal on OXTL. This can be provided by an external clock, or external components may be connected to the SD2015 internal oscillator.

5.4.1 Internal Oscillator Option

The oscillator cell will function with either a 460.8kHz crystal or ceramic resonator. Figure 9 illustrates the crystal option for clock generation using a parallel resonant crystal and two tuning capacitors. Capacitors values may depend on the recommendations of the resonator manufacturers. They are typically in the range of 33pF to 470pF.

5.4.2 External Clock Option

Figure 10 shows the external 460.8kHz clock source

option. Note that IXTL must be connected to V_{SS} in order to disable the internal oscillator.

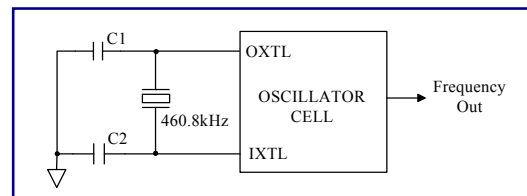


Figure 9. Crystal oscillator

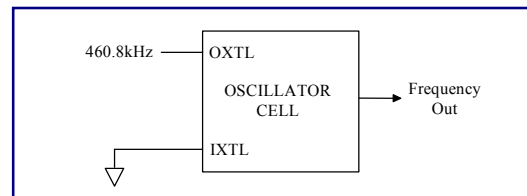


Figure 10. Oscillator with external clock

6.0 Electrical Specifications

Table 3. Absolute Maximums

Symbol	Parameter	Min.	Max.	Units
T _A	Ambient	-40	+85	°C
T _S	Storage temperature	-55	150	°C
V _{DD}	Supply voltage	-0.3	6.0	V
V _{IN} , V _{OUT}	DC input, output	-0.3	V _{DD} +0.3	V
T _L	Re-flow solder profile		Per IPC/JEDECJ-STD-020C	°C

Cautions: This integrated circuit can be damaged by ESD. It must be stored in conductive foam and handled with proper precaution. Stresses above absolute maximum ratings may result in damage to the device. Remove power before insertion or removal of this device.

Table 4. DC Characteristics

(V_{DD} = 3.0V to 5.5V, V_{SS} = 0V, T_A = -40°C to +85°C)

Symbol	Parameter	VDD	Min.	Typ.	Max.	Units
V _{IL}	Digital input voltage, logic 0	3.0-5.5			0.3*V _{DD}	V
V _{IH}	Digital input voltage, logic 1	3.0-5.5	0.7*V _{DD}			V
V _{OL}	Digital output voltage, logic 0 (I _{OL} =0.67mA)	3.0-5.5			0.4	V
V _{OH}	Digital output voltage, logic 1 (I _{OH} =0.67mA)	3.0-5.5	V _{DD} -0.6			V
C _{IN}	Input capacitance					pF
	Analog input			2.9		
	IRXA			25		
	Digital input			3.5		
I _{IL/IH}	Input leakage current				±500	nA
I _{OLL}	Output leakage current				±10	μA
I _{DD}	Power supply current	3.3		150	400	μA
		5.0		250	600	
IAREF	Analog reference	3.3	1.2	1.235	1.26	V
		5.0		2.5		
ICDREF*	Carrier detect reference (IAREF-0.08V)	3.3		1.155		V
		5.0		2.420		
OCBIAS	Circuit bias current (RBIAS=500k Ω, IAREF = 1.235V or RBIAS=1M Ω, IAREF = 2.5V)			2.5		μA

*The HART specification requires the carrier detect threshold to be between 80 to 120mVp-p. Setting ICDREF to 80mV below IAREF will set the carrier detect threshold to a nominal 100mVp-p.

Table 5. AC Characteristics

 ($V_{DD} = 3.0V$ to $5.5V$, $V_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$)

Pin Name	Description	Min.	Typ.	Max.	Units
IRXA	Analog receiver input				
	Leakage current			±150	nA
	Frequency - logic 1	1190	1200	1210	Hz
	Frequency - logic 0	2180	2200	2220	Hz
ORXAF	Analog receiver high pass filter output				
	Slew rate(SR)		0.025		V/μs
	Gain bandwidth (GBW)	500			kHz
	Voltage range	0.1		$V_{DD}-0.1$	V
IRXAC	Analog receiver filter and carrier detect comparators input				
	Leakage current			±500	nA
OTXA*	Analog modulator output				
	Frequency - logic 1		1200		Hz
	Frequency - logic 0		2200		Hz
	Amplitude (IAREF 1.235V)		500		mV _{P-P}
	Amplitude (IAREF 2.5V)		1000		mV _{P-P}
	Slope		2.79		mV/μs
	Loading	30			kΩ
	Inactive output (INRTS=logi1) VDD=3.3V		0.5		V
	Inactive output (INRTS=logi1) VDD=5V		1		V
ORXD	Receive digital output				
	Rise/fall time	20			ns
OCD	Carrier detect output				
	Rise/fall time	20			ns

*The modulator output frequencies are proportional to the input clock frequency (460.8kHz).

Table 6. Modem Characteristics

 ($V_{DD} = 3.0V$ to $5.5V$, $V_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$)

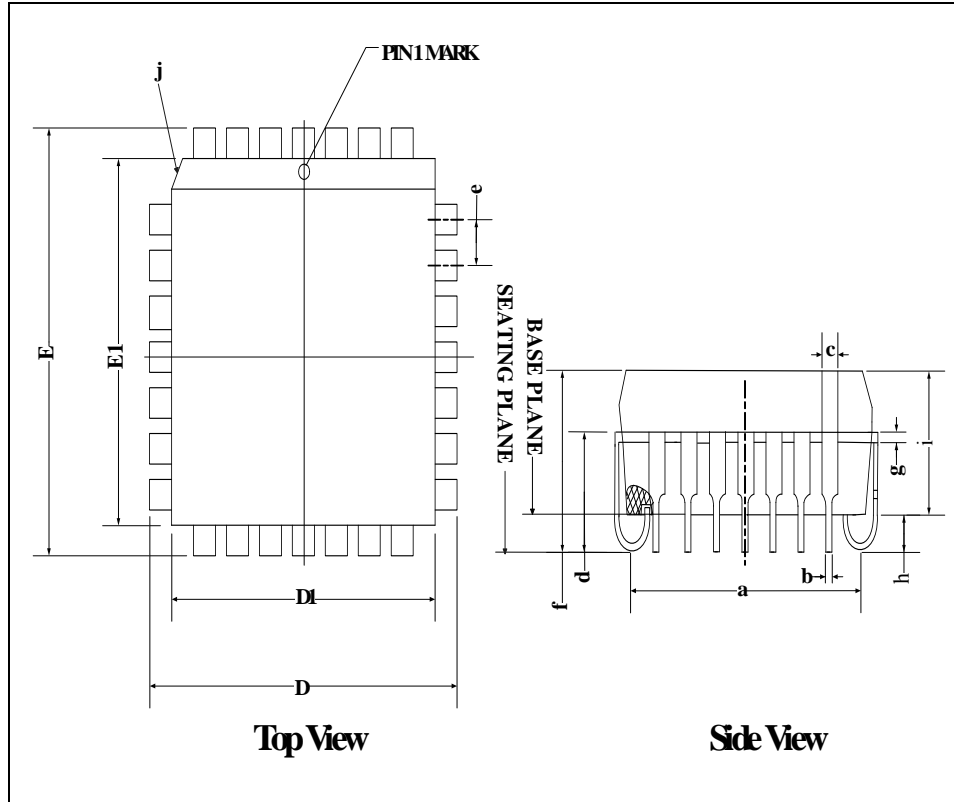
Parameter	Max.	Units
Demodulator jitter	12	% of 1 bit
Conditions:		
1. Input frequencies at 1200Hz ± 10Hz, 2200Hz ± 20Hz		
2. Clock frequency of 460.8kHz ± 0.1%		
3. Input (IRXA) asymmetry, 0		

Table7. Ceramic Resonator - External Clock Specifications

 ($V_{DD} = 3.0V$ to $5.5V$, $V_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$)

Parameter	Min.	Typ.	Max.	Units
Resonator				
Tolerance			±1.0	%
Frequency	460.8			kHz
External clock				
Clock frequency	456.2	460.8	465.4	kHz
Duty cycle	40	50	60	%
Amplitude		$V_{OH}-V_{OL}$		V

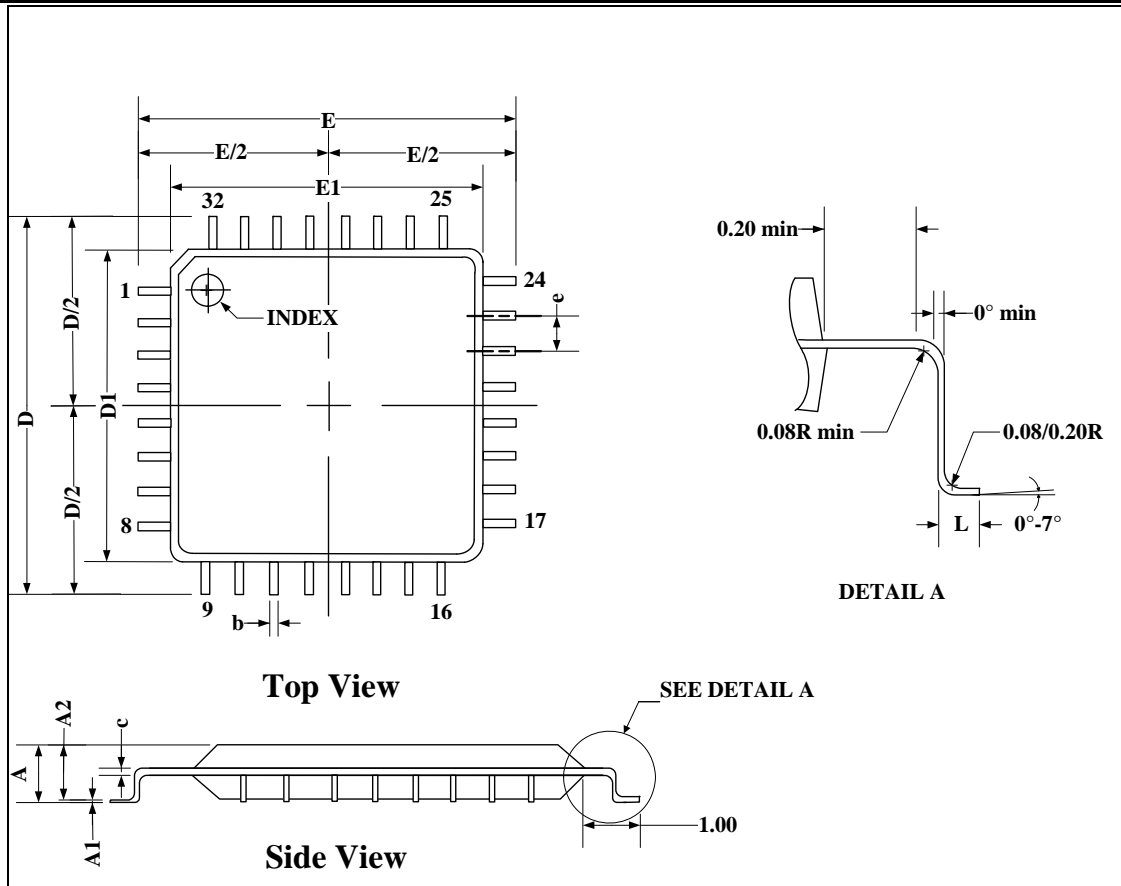
7.0 Mechanical Specifications



Dimensions: inches (mm)

Symbol	Min.	Nom.	Max.
E	0.4850 (12.320)	-	0.4950 (12.574)
E1	0.4500 (11.430)	-	0.4560 (11.582)
D	0.4850 (12.320)	-	0.4950 (12.574)
D1	0.4500 (11.430)	-	0.4560 (11.582)
a	0.3900(9.906)	-	0.4300 (10.922)
b	0.0130 (0.330)	-	0.0210 (0.533)
c	0.0260 (0.660)	-	0.0320 (0.813)
d	0.0900 (2.286)	-	0.1200 (3.048)
e	-	0.0500 (1.270)	-
f	0.1650 (4.191)	-	0.1800 (4.572)
g	0.0075 (0.191)	-	0.0125 (0.318)
h	0.0200 (0.508)	-	-
i	0.1480 (3.760)	-	0.1540 (3.912)
j	0.0420 (1.067) *45°		0.048 (1.219)*45°

Figure 11. 28 lead PLCC mechanical specification



Dimensions: mm

Symbol	Min.	Nom.	Max.
A	-	-	1.6
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
D		9.00	
D/2		4.50	
D1		7.00	
E		9.00	
E/2		4.50	
E1		7.00	
L	0.45	0.60	0.75
e		0.80	
b	0.30	0.37	0.45
c	0.09	-	0.20

Figure 12. 32 lead LQFP mechanical specification